Application Notes

(Preliminary)

Model: UG-2832GLBAT02

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Notes:

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Revised History

Part Number	Revision	Revision Content	Revised on
UG-2832GLBAT02	A	New	November 16, 2004

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Contents

1. Basic Specifications

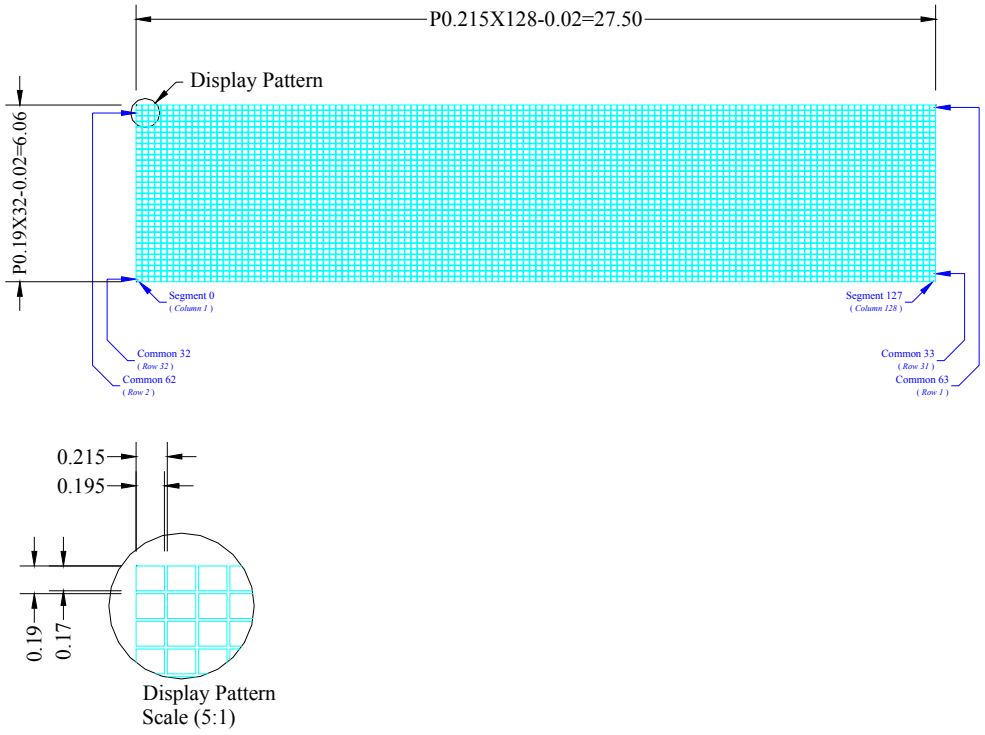
1.1 Display Specifications

1) Display Mode: Passive Matrix
2) Display Color: Monochrome (Light Blue)
3) Drive Duty: 1/32 Duty

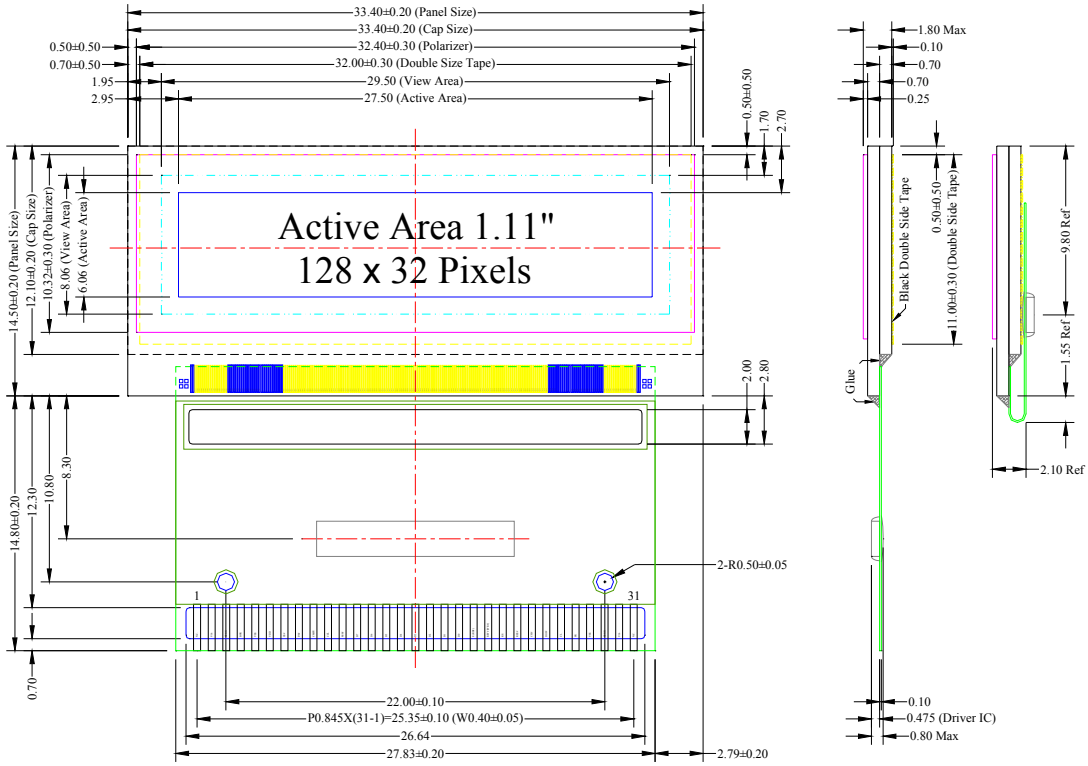
1.2 Mechanical Specifications

1) Outline Drawing: According to the annexed outline drawing number
2) Number of Pixels: 128 × 32
3) Panel Size: 33.40 × 14.50 × 1.80 (mm)
4) Active Area: 27.50 × 6.06 (mm)
5) Pixel Pitch: 0.215 × 0.19 (mm)
6) Pixel Size: 0.195 × 0.17 (mm)
7) Weight: TBD (g)

1.3 Active Area & Pixel Construction



1.4 Mechanical Drawing



General Tolerance: ±0.30
Unit: mm

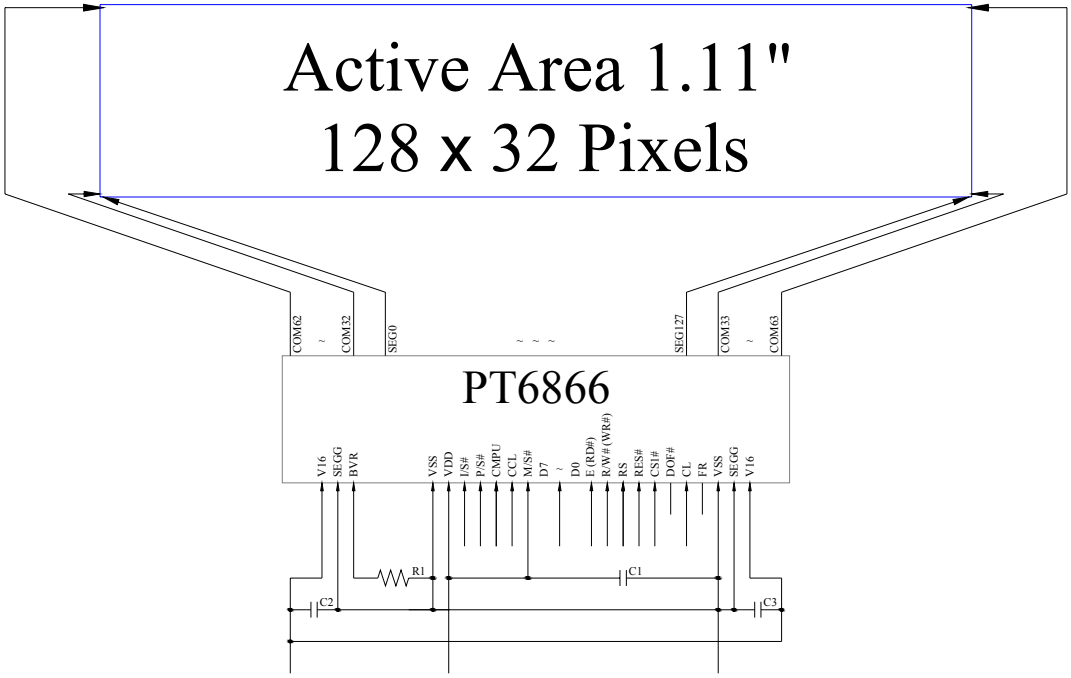
1.5 Pin Definition

<table>
<tr><th>Pin Number</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>6</td><td>VDD</td><td>I</td><td>Power Supply for Logic Circuit
This is a voltage supply pin. It must be connected to external source.</td></tr>
<tr><td>5, 28</td><td>VSS</td><td>I</td><td>Ground of OEL System
This is a ground pin. It also acts as a reference for the logic pins. It must be connected to external ground.</td></tr>
<tr><td>2, 30</td><td>V16</td><td>I</td><td>Power Supply for OEL Panel
This is the most positive voltage supply pin of the chip. It is supplied externally.</td></tr>
<tr><td>3, 29</td><td>SEGG</td><td>I</td><td>External Voltage Reference for Pre-charge Signal
This pin is the reference for OEL driving voltages. It is supplied externally.</td></tr>
<tr><td>4</td><td>BVR</td><td>I</td><td>Current Reference for Brightness Adjustment
This pin is segment current reference pin. A resistor should be connected between this pin and VSS.</td></tr>
<tr><td>10</td><td>CCL</td><td>I</td><td>Select Internal/External System Clock Source
This pin is internal clock enable. When this pin is pulled high, internal clock is enabled. The internal clock will be disabled when it is pulled low, an external clock source must be connected to CL pin for normal operation.</td></tr>
<tr><td>26</td><td>CL</td><td>I/O</td><td>External System Clock Source
This pin is the system clock input. When internal clock is enabled, this pin should be left open. Nothing should be connected to this pin. When internal clock is disabled, this pin receives display clock signal from external clock source.</td></tr>
<tr><td>11</td><td>M/S#</td><td>I</td><td>Master/Slave Select
This pin is the selection input. This pin must be pulled high to enable the chip function as master.</td></tr>
<tr><td>27
25</td><td>FR
DOF#</td><td>I/O</td><td>Cascade Application Connection Pin
These pins are No Connection pins. These should be left open individually.</td></tr>
<tr><td>7
8
9</td><td>I/S#
P/S#
CMPU</td><td>I</td><td>Communicating Protocol Select
These pins are MCU interface selection input. See the following table:
<table>
<tr><th></th><th>68XX-parallel</th><th>80XX-parallel</th><th>Serial</th><th>I2C</th></tr>
<tr><td>I/S#</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>P/S#</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>CMPU</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
</table></td></tr>
<tr><td>23</td><td>RES#</td><td>I</td><td>Power Reset for Controller and Driver
This pin is reset signal input. When the pin is low, initialization of the chip is executed.</td></tr>
<tr><td>24</td><td>CS1#</td><td>I</td><td>Chip Select
This pin is the chip select input. The chip is enabled for MCU communication only when CS1# is pulled low.</td></tr>
</table>

1.5 Pin Definition (Continued)

Pin Number	Symbol	I/O	Function
20	E (RD#)	I	*Read/Write Enable or Read* This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the chip is selected. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and chip is selected.
21	R/W# (WR#)	I	*Read/Write Select or Write* This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled high and write mode when low. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the chip is selected.
22	RS	I	*Data/Command Control* This pin is Data/Command control pin. When the pin is pulled high, the data at D7~D0 is treated as display data. When the pin is pulled low, the data at D7~D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.
12~19	D7~D0	I/O	*Host Data Input/Output Bus* These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D7 will be the serial data input (SDA) and D6 will be the serial clock input (SCK). When I2C mode is selected, D6 will be the clock signal (SCL) and D7 will be the I2C data input (SDA). Refer to the configuration of I2C interface.
1, 31	N.C.	-	*Reserved Pin (Supporting Pin)* The supporting pins can reduce the influences from stresses on the function pins.

1.6 Block Diagram



MCU Interface Selection: I/S#, P/S# and CMPU
Pins connected to MCU interface:
D7~D0, E (RD#), R/W# (WR#), RS, RES#, and CS1#

C1: 4.7μF
C2, C3: 10μF
R1: 130kΩ

2. Absolute Maximum Ratings

2.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage	V_{DD}	-0.3	4.0	V	1, 2
Driver Supply Voltage	V_{16}	0	15	V	1, 2
Operating Temperature	T_{OP}	-20	70	°C	-
Storage Temperature	T_{STG}	-30	80	°C	-

Note 1: All the above voltages are on the basis of "GND = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

2.2 Regarding the Gradation

Although this module possesses the gradation function, respective gradation levels will vary depending on the production conditions etc. Also, the temperature range where the gradation function can be guaranteed will be -10°C~60°C.

3. Electrical Characteristics

3.1 DC Characteristics

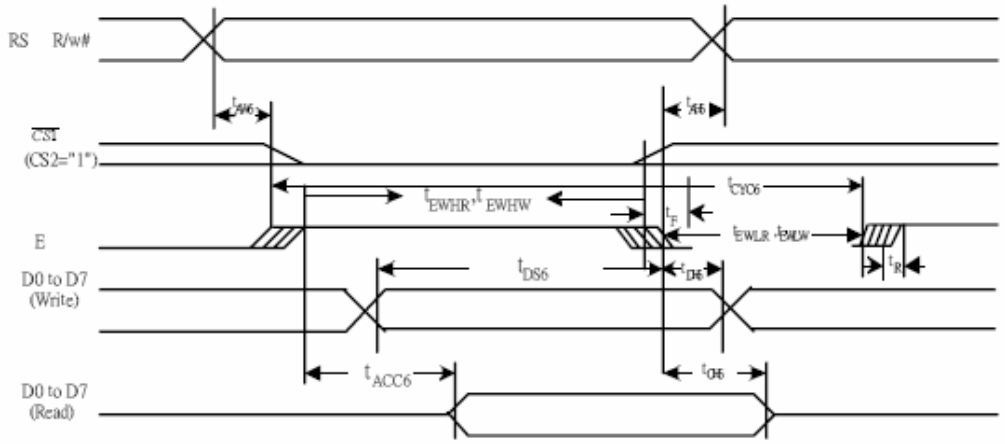
Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.4	2.8	3.5	V
Driver Supply Voltage	V_{16}		-	7.5	-	V
High Level Input	V_{IH}	I_{out} = 100μA, 3.3MHz	0.8×V_{DD}	-	V_{DD}	V
Low Level Input	V_{IL}	I_{out} = 100μA, 3.3MHz	0	-	0.2×V_{DD}	V
High Level Output	V_{OH}	I_{out} = 100μA, 3.3MHz	0.9×V_{DD}	-	V_{DD}	V
Low Level Output	V_{OL}	I_{out} = 100μA, 3.3MHz	0	-	0.1×V_{DD}	V

3.2 AC Characteristics

3.2.1 68XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{AH6}	Address Hold Time	10	-	ns
t_{AW6}	Address Setup Time	20	-	ns
t_{CYC6}	System Cycle Time	300	-	ns
t_{DS6}	Write Data Setup Time	40	-	ns
t_{DH6}	Write/Read Data Hold Time	15	-	ns
t_{ACC6}	Access Time	-	140	ns
t_{OH6}	Output Disable Time	-	70	ns
t_{EWHR} t_{EWHW}	Enable High Pulse Time (Read) Enable High Pulse Time (Write)	120 60	-	ns
t_{EWLR} t_{EWLW}	Enable Low Pulse Time (Read) Enable Low Pulse Time (Write)	120 60	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

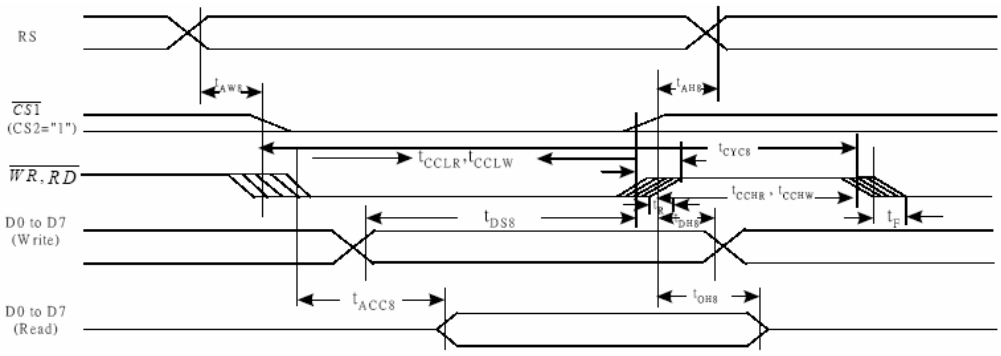
* All the timings should be based on 30% and 70% of V_{DD}-GND.



3.2.2 80XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{AH8}	Address Hold Time	10	-	ns
t_{AW8}	Address Setup Time	20	-	ns
t_{CYC8}	System Cycle Time	300	-	ns
t_{DS8}	Write Data Setup Time	40	-	ns
t_{DH8}	Write/Read Data Hold Time	15	-	ns
t_{ACC8}	Access Time	-	140	ns
t_{OH8}	Output Disable Time	-	70	ns
t_{CCHR} t_{CCHW}	Control High Pulse Width (Read) Control High Pulse Width (Write)	120 60	-	ns
t_{CCLR} t_{CCLW}	Control Low Pulse Width (Read) Control Low Pulse Width (Write)	120 60	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

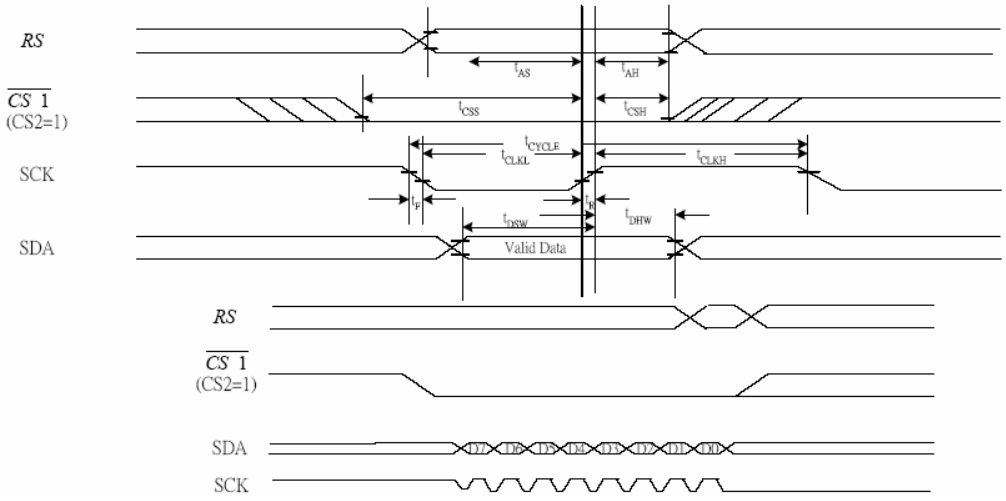
* All the timings should be based on 30% and 70% of V_{DD}-GND.



3.2.3 Serial Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	ns
t_{AS}	Address Setup Time	150	-	ns
t_{AH}	Address Hold Time	150	-	ns
t_{CSS}	Chip Select Setup Time	120	-	ns
t_{CSH}	Chip Select Hold Time	60	-	ns
t_{DSW}	Write Data Setup Time	100	-	ns
t_{DHW}	Write Data Hold Time	100	-	ns
t_{CLKL}	Clock Low Time	100	-	ns
t_{CLKH}	Clock High Time	100	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

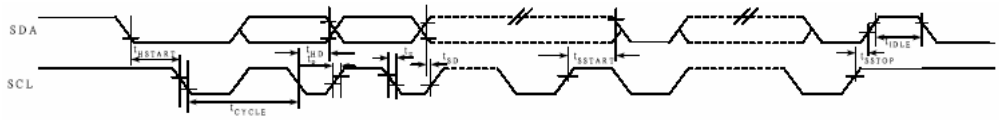
* All the timings should be based on 30% and 70% of V_{DD}-GND.



3.2.4 I^2C Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	μs
t_{HSTART}	Start Condition Hold Time	0.6	-	μs
t_{HD}	Data Hold Time	300	-	ns
t_{SD}	Data Setup Time	100	-	ns
t_{SSTART}	Start Condition Setup Time (Only Relevant for a Repeated Start Condition)	0.6	-	μs
t_{SSTOP}	Stop Condition Setup Time	0.6	-	μs
t_R	Rise Time for Data and Clock Pin	-	300	ns
t_F	Fall Time for Data and Clock Pin	-	300	ns
t_{IDLE}	Idle Time before a New Transmission Can Start	1.3	-	μs

* All the timings should be based on 30% and 70% of V_{DD}-GND.



3.3 General Electrical Specification

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.4	2.8	3.5	V
Driver Supply Voltage	V_{16}		7.0	7.5	8.5	V
Operating Current for V_{DD}	I_{DD}	Note 3	-	TBD	TBD	μA
		Note 4	-	TBD	TBD	μA
Operating Current for V_{16}	I_{16}	Note 3	-	TBD	TBD	mA
		Note 4	-	TBD	TBD	mA
Sleep Mode Current for V_{DD}	$I_{DD, SLEEP}$		-	TBD	-	μA
Sleep Mode Current for V_{16}	$I_{16, SLEEP}$		-	TBD	-	μA

Note 3: V_{DD} = 2.8V, V_{16} = 7.5V, Frame Rate = 150Hz, Brightness Setting = 0xFF, 50% Display Area Turn on.

Note 4: V_{DD} = 2.8V, V_{16} = 7.5V, Frame Rate = 150Hz, Brightness Setting = 0xFF, 100% Display Area Turn on.

4. Functional Specification

4.1. Commands

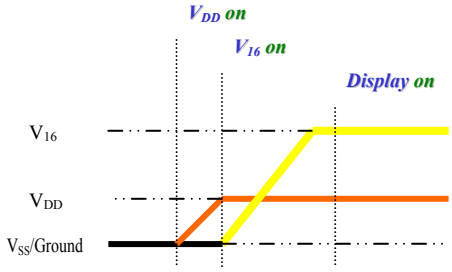
Refer to the Technical Manual for the PT6866

4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

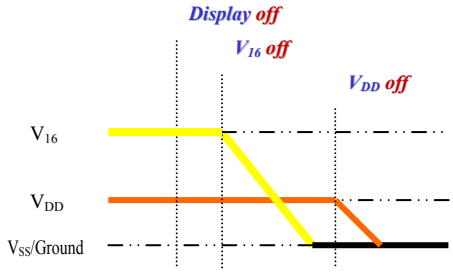
4.2.1 Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Clear Screen
4. Power up V_{16}
5. Delay 100ms
   (when V_{DD} is stable)
6. Send Display on command



4.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{16}
3. Delay 100ms
   (when V_{16} is reach 0 and panel is completely discharges)
4. Power down V_{DD}



4.3 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 132×(64+1) [Included ICONS line] Display Mode
3. Normal segment and display data column address mapping (SEG0 mapped to address 00H, ADC is forward.)
4. Normal display
5. Read-modify-write mode is OFF
6. Display start line is set at display RAM address 0
7. Column address counter is set at 0
8. Page address is set at 0
9. Normal scan direction of the COM outputs
10. Power-saving mode is cleared
11. Serial interface is cleared
12. Brightness control register is set at level 80H
13. Pre-charge period is set at 8

14. Zero period is set at 8
15. Display offset is set to COM0

4.4 Actual Application Example

Command usage and explanation of an actual example

<Initialization Setting>
Software Reset
(11100010)

Set End of Read-Modify-Write Mode
(11101110)

Set Display Offset
(11010011 with **XXXXXX)
* XXXXXX = 64 - Dummy Lines from Common 0
Set Multiplex Ratio
(10101000 with **XXXXXX)

Set Frame Frequency
(10101010 with *10XXXXX)

Set Icon Mode (1101000X)
11010000 => 0xD0 (Off)

Set Pre-charge Period
(11011001 with XXXXXXXX)

Set Bias Current Mode
(10101011 with 10X0X00X)

Set Low Power Display Mode
(11011000 with 00000X0X)

Set Current Mode
(11011010 with ***1**X0)

Set Display Start Line
(01XXXXXX)
Set Segment Re-map (ADC Select)
(1010000X)
Set COM Output Scan Direction
(1100X***)

Set Brightness Control Register
(10000001 with XXXXXXXX)

Set Entire Display On/Off (1010010X)
10100100 => 0xA4 (Normal)

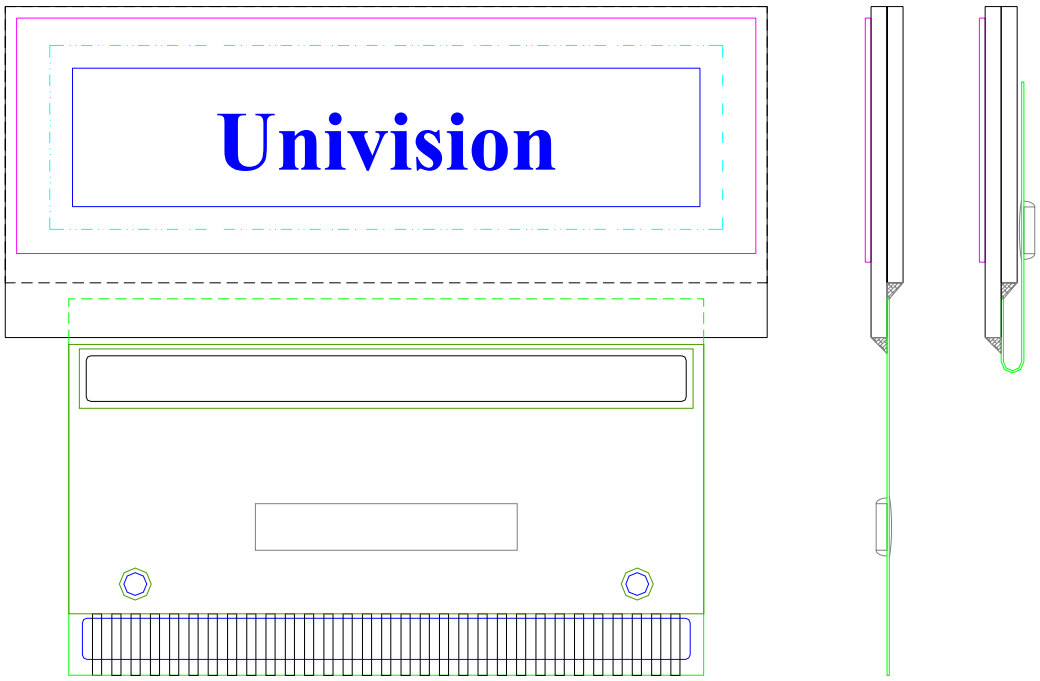
Set Normal/Inverse Display (1010011X)
10100110 => 0xA6 (Normal)
Set Display On/Off (1010111X)
10101111 => 0xAF (Turns On)

<Display Boundary Setting>
Set Page Address (1011XXXX)
10110000 => 0xB0
Set Lower Column Address
(0000XXXX)
Set Higher Column Address
(0001XXXX)

If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

5. Display Direction Setting

5.1 Normal Display Mode

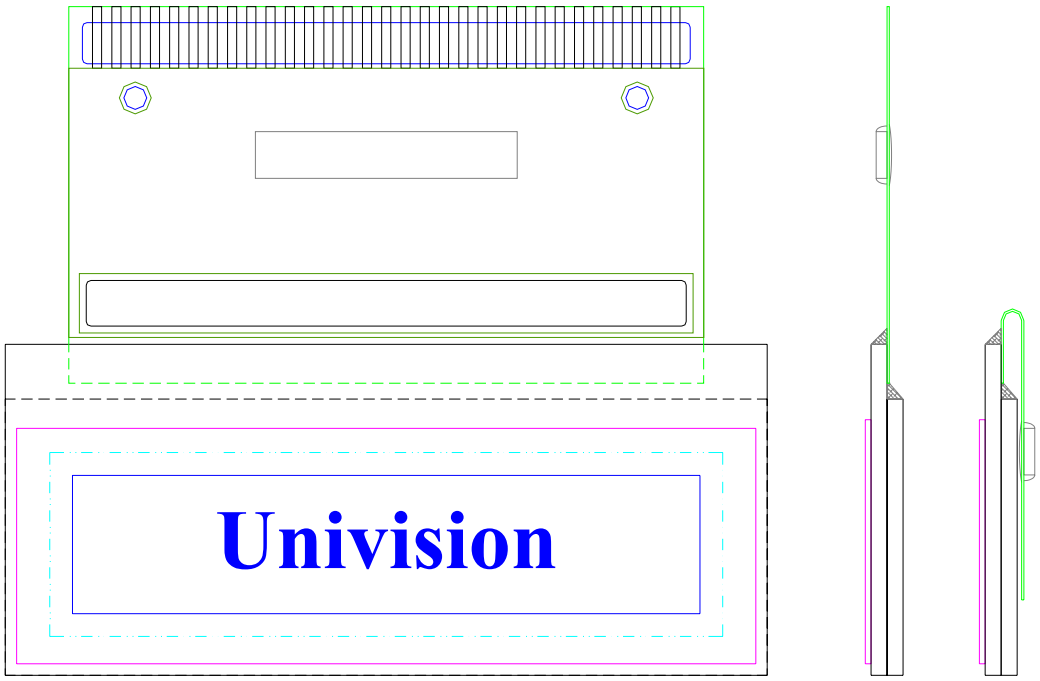


<Relative Instruction Setting>

Set Display Offset
0xD3 with 0x20
Set Multiplex Ratio
0xA8 with 0x1F
Set Display Start Line
0x40
Set Segment Re-map (ADC Select)
0xA0 (Rightward Output)
Set COM Output Scan Direction
0xC8 (Reverse Direction)

Set Lower Column Address
0x00
Set Higher Column Address
0x10

5.2 Inverted Display Mode



* The pattern shown in active area is the same as that in normal display mode but setting the COM Output Scan Direction as remapped mode.

<Relative Instruction Setting>

Set Display Offset
0xD3 with 0x20

Set Multiplex Ratio
0xA8 with 0x1F

Set Display Start Line
0x40

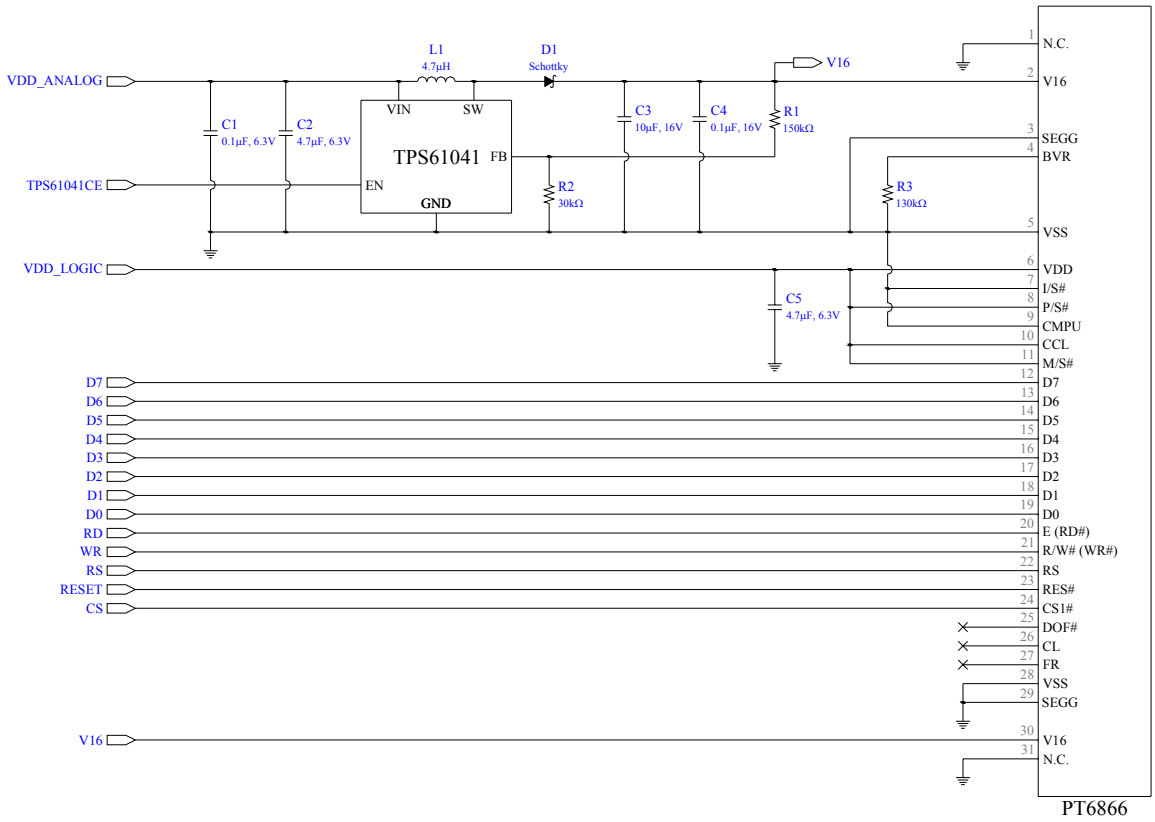
Set Segment Re-map (ADC Select)
0xA1 (Leftward Output)

Set COM Output Scan Direction
0xC0 (Normal Direction)

Set Lower Column Address
0x04

Set Higher Column Address
0x10

6. Application Circuit



8-bit 80XX Parallel Interface

DC/DC Converter: TPS61041
* TPS61041CE could be connected to MCU or VDD for alternative solution.
VCC = 1.233 × (R1 + R2) / R2

7. Components List

Item	Silk Name	Value	Remark
Driver IC	PT6866		(*PTC*)
DC/DC Converter	TPS61041		Step-up Type (*TI*)
Inductor	L1	4.7μH	2A
Schottky Diode	D1		1A, 20V
Resistor	R1	150kΩ	1%, 1/4W
	R2	30kΩ	1%, 1/4W
	R3	910kΩ	1%
Capacitor	C1	0.1μF	6.3V, Low ESR
	C2, C5	4.7μF	6.3V, Low ESR
	C3	10μF	16V, Low ESR
	C4	0.1μF	16V, Low ESR
	C6	4.7μF	16V, Low ESR

8. Precautions When Using These OEL Display Modules

8.1 Handling Precautions

1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If pressure is applied to the display surface or its neighborhood of the OEL display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
4) The polarizer covering the surface of the OEL display module is soft and easily scratched. Please be careful when handling the OEL display module.
5) When the surface of the polarizer of the OEL display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
   * Scotch Mending Tape No. 810 or an equivalent

   Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.

   Also, pay attention that the following liquid and solvent may spoil the polarizer:
   * Water
   * Ketone
   * Aromatic Solvents
6) When installing the OEL display module, be careful not to apply twisting stress or deflection stress to the OEL display module. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.
7) Do not apply stress to the LSI chips and the surrounding molded sections.
8) Do not disassemble nor modify the OEL display module.
9) Do not apply input signals while the logic power is off.
10) Pay sufficient attention to the working environments when handing OEL display modules to prevent occurrence of element breakage accidents by static electricity.
    * Be sure to make human body grounding when handling OEL display modules.
    * Be sure to ground tools to use or assembly such as soldering irons.
    * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
    * Protective film is being applied to the surface of the display panel of the OEL display module. Be careful since static electricity may be generated when exfoliating the protective film.
11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OEL display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
12) If electric current is applied when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

8.2 Storage Precautions

1) When storing OEL display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps, etc. and, also, avoiding high temperature and high humidity environments or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Univision Technology Inc.)
   At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
2) If electric current is applied when water drops are adhering to the surface of the OEL display module, when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

8.3 Designing Precautions

1) The absolute maximum ratings are the ratings which cannot be exceeded for OEL display module, and if these values are exceeded, panel damage may be happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
5) As for EMI, take necessary measures on the equipment side basically.
6) When fastening the OEL display module, fasten the external plastic housing section.
7) If power supply to the OEL display module is forcibly shut down by such errors as taking out the main battery while the OEL display panel is in operation, we cannot guarantee the quality of this OEL display module.
8) The electric potential to be connected to the rear face of the IC chip should be as follows: PT6866
   * Connection (contact) to any other potential than the above may lead to rupture of the IC.

8.4 Precautions when disposing of the OEL display modules

1) Request the qualified companies to handle industrial wastes when disposing of the OEL display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

8.5 Other Precautions

1) When an OEL display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.
   Nonetheless, if the operation is interrupted and left unused for a while, normal

state can be restored. Also, there will be no problem in the reliability of the module.

2) To protect OEL display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OEL display modules.
   * Pins and electrodes
   * Pattern layouts such as the TCP
3) With this OEL display module, the OEL driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OEL driver is exposed to light, malfunctioning may occur.
   * Design the product and installation method so that the OEL driver may be shielded from light in actual usage.
   * Design the product and installation method so that the OEL driver may be shielded from light during the inspection processes.
4) Although this OEL display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.