Princeton Technology Corp.
Tel: 886-2-66296288
Fax: 886-2-29174598
URL: http://www.princeton.com.tw

DESCRIPTION

PT6866 is a single-chip CMOS OLED driver with a controller for O/PLED (organic/polymer light emitting diode) dot-matrix graphic display systems. PT6866 consists of 132 high voltage/current driving output pins for driving 132 segments and 64 commons plus 1 icon line driving common. This IC is designed for Common Cathode type OLED panels.

PT6866 displays data directly from its internal 132x65 bit GDDRAM (Graphic Display Data RAM). Data/Commands are sent from the general MCU through a pin-selectable 6800- or 8080-series compatible Parallel Interface, a Serial Peripheral Interface, or I^2C Interface.

PT6866 reduces the number of external components by including a brightness control function and an on-chip oscillator.

FEATURES

- Supports max. 132x(64+1) matrix panel
- Power supply to logic system: 2.4V-5V
- Power supply to OLED system: 7.0V-16V
- Segment output maximum current: 400uA
- Common sink maximum current: 40mA
- Half range and full range current mode selection
- LOW current sleep mode (<5.0uA)
- External current reference control by external resistor
- 256-step brightness control on monochrome passive OLED panel
- On-Chip Oscillator
- Programmable Frame Rate
- 8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface, Serial Peripheral Interface and I^2C Interface
- Embedded 132x65 bit SRAM display buffer
- Row and Column re-mapping
- Vertical scrolling
- Supports Partial display
- COF and Gold Bump Chip available

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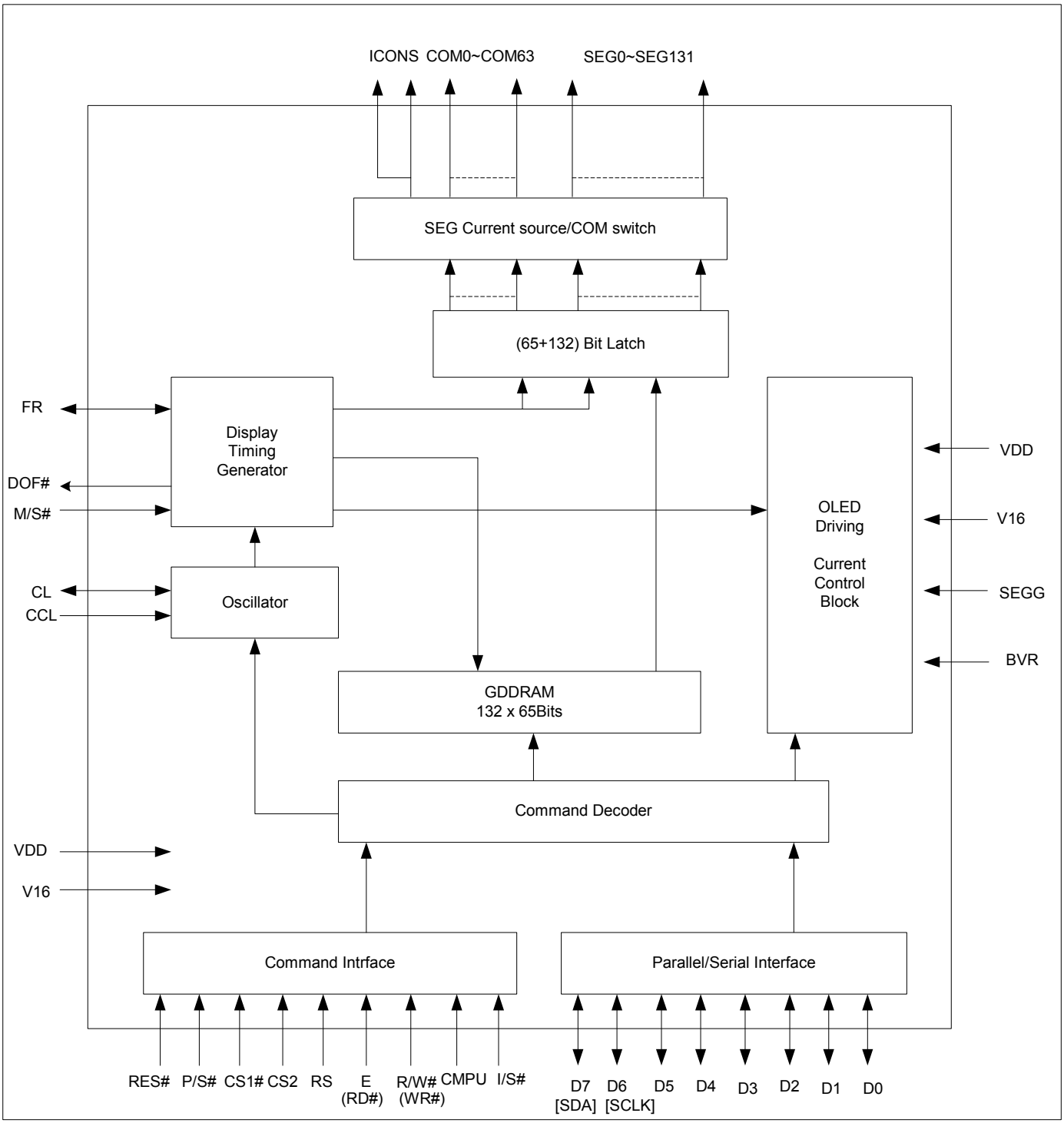
BLOCK DIAGRAM



PIN DESCRIPTION

FR, DOF#
These pins are No Connection pins. These pins should be left open individually.

CL
This pin is the system clock input. When internal clock is enabled, this pin should be left open. Nothing should be connected to this pin. When internal oscillator is disabled, this pin receives display clock signal from external clock source.

CS1#, CS2
These pins are the chip select inputs. The chip is enabled for MCU communication only when CS1# is pulled LOW and CS2 is pulled HIGH.

RES#
This pin is reset signal input. When the pin is LOW, initialization of the chip is executed.

RS
This pin is Data/Command control pin. When the pin is pulled HIGH, the data at D7-D0 is treated as display data. When the pin is pulled LOW, the data at D7-D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.

R/W#(WR#)
This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected.

E (RD#)
This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected. When connecting to an 8080-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled LOW and the chip is selected.

D7-D0
These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D7 will be the serial data input (SDA) and D6 will be the serial clock input (SCK). When I^2C mode is selected, D6 will be the clock signal (SCL) and D7 will be the I^2C data input (SDA). Refer to the configuration of I^2C interface.

SEGG
This pin is reference voltage, which is used to deliver a reference voltage for Seg Cells. The pin should be connected to V_{SS}.

V_{DD} Power Supply Pin
This is also the reference for the OLED driving voltages. It must be connected to external source.

V_{SS} Ground
It also acts as a reference for the logic pins. It must be connected to external ground.

V16
This is the most positive voltage supply pin of the chip. It is supplied externally.

M/S#
This pin is the selection input. This pin must be pulled HIGH; the chip function is as master.

CCL
This pin is internal clock enable. When this pin is pulled HIGH, internal clock is enabled. The internal clock will be disabled with it is pulled LOW; an external clock source must be connected to CL pin for normal operation.

CMPU
This pin is MCU parallel interface selection input. When the pin is pulled HIGH, 6800 series interface is selected and when the pin is pulled LOW, 8080 series interface is selected. If Serial Interface is selected (P/S# pulled LOW), the setting of this pin is ignored, but must be connected to a known logic (either HIGH or LOW).

P/S#
This pin is parallel interface selection input. When this pin is pulled HIGH, parallel interface mode is selected. When this pin and I/S# pins are pulled LOW, serial peripheral interface is selected.
Note: Read data operation is only available in parallel mode.

I/S#
This pin is serial interface selection input. When this pin pulled HIGH and P/S# pulled LOW, I^2C interface is selected.

COM0-COM63
These pins provide the Common switch signals to the OLED panel.

SEG0-SEG131
These pins provide the OLED segment driving signals. The output voltage level of these pins is in HIGH impedance stage when display is OFF.

ICONS

There are two ICONS pin on the chip. They are the common pins for the icon row. Both pins output exactly the same signal. The reason for duplicating the pin is to enhance the flexibility of the OLED layout.

BVR

This pin is current reference pin. A resistor (130KΩ) should be connected between this pin and VSS.

FUNCTIONAL BLOCK DESCRIPTION

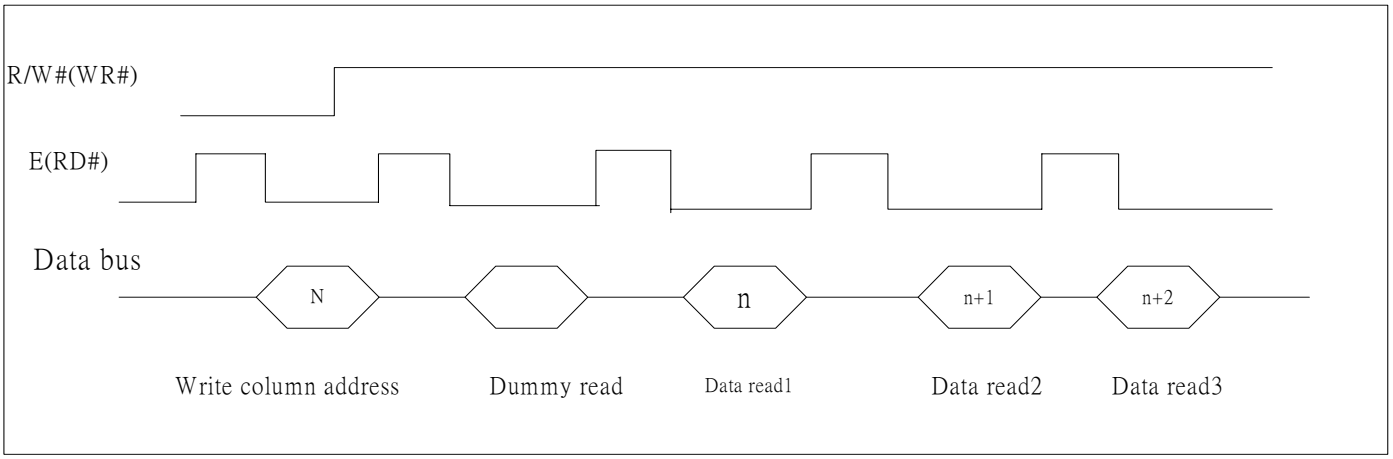
COMMAND DECODER AND COMMAND INTERFACE

This module determines whether the input data is interpreted as data or a command. Data is interpreted based upon the input of the RS pin. If the RS pin is HIGH, data is written to GDDRAM. If it is LOW, the input at D7-D0 is interpreted as a command and will be decoded and written to the corresponding command register.

MPU PARALLEL 6800-SERIES INTERFACE

The parallel interface consists of 8 bi-directional data pins (D0-D7), R/W# (WR#), RS, E (RD#), CS1# and CS2. RW# (WR#) HIGH input indicates a read operation from the GDDRAM or the status register. RW# (WR#) LOW input indicates a write operation to Display Data RAM or Internal Command Registers, depending on the status of the RS input.

The E (RD#) input serves as a data latch signal (clock) when HIGH, provided that CS1# and CS2 are LOW and HIGH respectively. In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is performed internally which requires the insertion of a dummy read before the first actual display data read. This is shown in the below.



Display data read back procedure-insertion of dummy read

MPU PARALLEL 8080-SERIES INTERFACE

The Parallel interface consists of 8 bi-directional data pins (D7-D0), E (RD#), R/W# (WR#), RS, CS1# and CS2. The E (RD#) input serves as data read latch signal (clock) when LOW, provided that CS1# and CS2 are LOW and HIGH respectively.

Display data or status register read is controlled by RS.R/W# (WR#) input serves as data write latch signal (clock) when HIGH provided that CS1# and CS2 are LOW and HIGH respectively.

Display data or command register write is controlled by RS (refer to timing characteristics for Parallel Interface Timing Diagram of 8080-series microprocessor). Similar to the 6800-series interface, a dummy read is also required before the first actual display data read.

MPU SERIAL PERIPHERAL INTERFACE

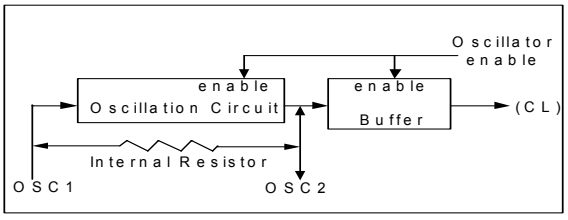
The serial peripheral interface consists of serial clock SCK, serial data SDA, RS, CS1# and CS2. SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6,…..D0, RS is sampled on every eighth clock and the data byte in the shift register is written to the Display Data RAM or command register in the same clock.

MPU I^2C INTERFACE

I^2C-bus data signal SDA and I^2C-bus clock signal SCL. The data signal must be connected to pull-up resistor. There are also five input signals including, RES#, CS1#, CS2, P/S#, I/S#, which is used for the initialization of device.

OSCILLATOR CIRCUIT

The below is an On-Chip LOW power RC oscillator circuitry. The oscillator generates the clock for the Display Timing Generator.



Oscillator circuit

OLED DRIVING CURRENT CONTROL BLOCK

This block is used to divide the incoming power sources into the different levels of internal use voltage and current. V16 and V_{DD} are external power supplies. SEGG is reference voltage, which is used to deliver a reference voltage for Seg Cells. BVR is a reference current source for Seg Cells current drivers.

GDDRAM

The GDDRAM is bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 132×65=8580 bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display.

197 BIT LATCH

A register carries the display signal information. In 132×65 display mode, data will be fed to the Seg/Com Cell and output to the required voltage/current level respectively.

SEG/COM CELL

Seg current source drives deliver 132 current sources to drive OLED panel. It uses current source to drive the Seg Cell where the driving current can be adjusted by 256 steps.

COMMAND TABLE

(Based on the 80 port MPU; the RD and WR commands differ for the 68 port MPU)

Command		RDB	WRB	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
<1>	Display ON/OFF	1	0	0	1	0	1	0	1	1	1	0/1	Switch the entire display ON or OFF, regardless of the Display RAM's data or the internal status. 1:ON 0:OFF (POR)*1, (power save)*
<2>	Display Start Line Set	1	0	0	0	1	Display START address (0-63)						Determine the line of RAM data to be displayed at the display's top line [COM0]. (POR)*6
<3>	Page Address Set	1	0	0	1	0	1	1	Page (0-8)				Set the page of the Display RAM in the page address register. (POR)*8
<4>	LOWer Column (segment) Address Set	1	0	0	0	0	0	0	LSB Column Address				Set the LSB column address of the Display RAM in the column address register. Column Address is composed of 8 bits.
<5>	HIGHer Column (segment) Address Set	1	0	0	0	0	0	1	MSB Column Address				Set the MSB column address of the Display RAM in the column address register. Column Address(0-131), (POR)*7
<6>	Status Read	0	1	0	BUSY	ACC	ON/OFF	RESET	0	0	0	0	Read the status. Busy 1: Busy (internal processing) 0: Ready status ADC 1: Rightward (forward) Output 0: Leftward (reverse) Output ON/OFF 1: Display OFF. 0: Display ON RESET 1: Resetting. 0: Normal
<7>	Display Data Write	1	0	1	Write Data								Write the data on the data bus to RAM. These commands access a previously-specified address of the Display RAM, after which the column address is incremented by one.
<8>	Display Data Read	0	1	1	Read Data								Read data from the Display RAM onto the data bus.
<9>	Multiplex Ratio Set	1	0	0	1	0	1	0	1	0	0	0	Double byte command
		1	0	0	x	x	Ratio Factor (0-63)						Select multiplex duty Max. ratio : 65(POR) ; SN=RF+2
<10>	Frame Frequency Set	1	0	0	1	0	1	0	1	0	1	0	Double byte command
					x	1	0	0	0	0	0	1	Fosc/(4*DF)
					x	1	0	0	0	0	1	0	Fosc/(6*DF) for DF=65(POR)
					x	1	0	0	0	0	1	1	Fos/(8*DF)
<11>	COM Output Mode Select	1	0	0	1	1	0	0	0/1	x	x	x	Select COM output scan direction 0:Normal Direction (POR)*9 + 1:Reverse Direction
<12>	ADC Select	1	0	0	1	0	1	0	0	0	0	0/1	Used to reverse the correspondence between the Display RAM's column address and segment driver output ports 0: Rightward (forward)output (POR)*3 + 1: Leftward (reverse) output
<13>	Static Drive ON/OFF	1	0	0	1	0	1	0	0	1	0	0/1	Select normal display operation or static all-lit drive display operation. 1: Static drive (power save)* 0: Normal display (POR)*4
<14>	Brightness Set	1	0	0	1	0	0	0	0	0	0	1	Double byte command
		1	0	0	Brightness Level (0-255)								Select the brightness factor for driving OLED cells. Brightness Level : 128 (POR)*12
<15>	Read Modify Write	1	0	0	1	1	1	0	0	0	0	0	Increase column address counter by 1 when display is written. (This is not done when data is read)

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Command		RDB	WRB	RS	D7	D6	D5	D4	D3	D2	D1	D0	Function
<16>	End	1	0	0	1	1	1	0	1	1	1	0	Cancel the Read Modify Write mode. (POR)*5
<17>	Reset	1	0	0	1	1	1	0	0	0	1	0	Reset the Display Start Line to the 1st line in the register. Resets the column address counter to 0 and page address to 0. Read modify write mode is OFF. COM scan is normal direction.
<18>	Icon Mode Set	1	0	0	1	1	0	1	0	0	0	0/1	0:Icon mode OFF (POR)*2 1:Icon mode ON
<19>	Display Mode Set	1	0	0	1	0	1	0	0	1	1	0/1	0:Normal display (POR)*4 1:inverse display
<20>	Current Mode Set	1	0	0	1	1	0	1	1	0	1	0	Double byte command
		1	0	0	x	x	x	1	x	x	0/1	0	0:half range current mode (POR) 1:full range current mode
<21>	Pre-charge & Zero Period Select	1	0	0	1	1	0	1	1	0	0	1	Double byte command
		1	0	0	Pre-charge Period (0~15) Invalid entry is 0				Zero Period (0~15) Invalid entry is 0				Pre-charge period (POR)*13
													Zero period (POR)*14
<22>	Bias Current	1	0	0	1	0	1	0	1	0	1	1	Double byte command
		1	0	0	1	0	0	0	1	0	0	0	Normal (POR)
					1	0	1	0	0	0	0	1	LOW Bias Current Mode
<23>	Display Offset	1	0	0	1	1	0	1	0	0	1	1	Double byte command
		1	0	0	x	x	Scroll row number (0-63)						Com output sequence (POR)*15
<24>	LOW Power Display	1	0	0	1	1	0	1	1	0	0	0	Double byte command
		1	0	0	0	0	0	0	0	0	0	0	Normal (POR)
					0	0	0	0	0	1	0	1	LOW power consumption
<25>	NOP	1	0	0	1	1	1	0	0	0	1	1	Command for NO Operation

Notes:
* With display OFF (command <1>), static drive on (command <13>) invokes power-saving mode.
* For power-saving mode (sleep mode)
  1. Sleep mode can be exited by the issue of a new software command.
  2. Internal oscillator is stopped
  3. OLED power supply circuits is turned OFF
  4. Segment and Common drivers output HIGH impedance level
  5. The display data and operation mode before sleep are held
  6. Internal display RAM can still be accessed
* When the power is turned on, the IC internal state becomes unstable, and it is necessary to initialize it using the RES# terminal. When RES# input is LOW the chip is initialized as follows:
  1. Display is OFF
  2. 132x(64+1) Display Mode
  3. ADC is Forward
  4. Normal display
  5. Read Modify Write is OFF
  6. Display start line is set at display RAM address 0
  7. Column address counter is set at 0
  8. Page address is set at 0
  9. COM scan is normal direction
  10. Power-saving mode is cleared
  11. Serial interface is cleared

12. Brightness register is set at Level 10000000
13. Pre-charge period is set at 1000
14. Zero period is set at 1000
15. Display offset is set to COM0

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PIN ASSIGNMENTS

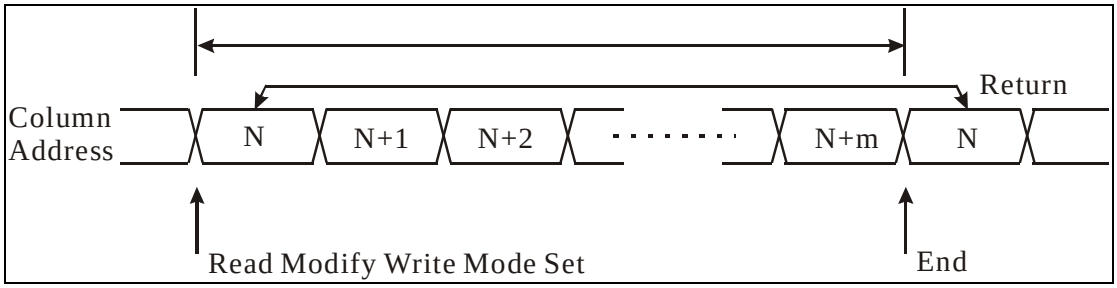
COM pin assignments for COM signals in Programmable Multiplex Ratio

Die Pad Name	64 Mux Com Signal Output	54 Mux Com Signal Output	53 Mux Com Signal Output	49 Mux Com Signal Output	48 Mux Com Signal Output	33 Mux Com Signal Output	32 Mux Com Signal Output	16 Mux Com Signal Output
COM0	COM0	COM0	COM0	COM0	COM0	COM0	COM0	COM0
COM1	COM1	COM1	COM1	COM1	COM1	COM1	COM1	COM1
COM2	COM2	COM2	COM2	COM2	COM2	COM2	COM2	COM2
COM3	COM3	COM3	COM3	COM3	COM3	COM3	COM3	COM3
COM4	COM4	COM4	COM4	COM4	COM4	COM4	COM4	COM4
COM5	COM5	COM5	COM5	COM5	COM5	COM5	COM5	COM5
COM6	COM6	COM6	COM6	COM6	COM6	COM6	COM6	COM6
COM7	COM7	COM7	COM7	COM7	COM7	COM7	COM7	COM7
COM8	COM8	COM8	COM8	COM8	COM8	COM8	COM8	COM8
COM9	COM9	COM9	COM9	COM9	COM9	COM9	COM9	COM9
COM10	COM10	COM10	COM10	COM10	COM10	COM10	COM10	COM10
COM11	COM11	COM11	COM11	COM11	COM11	COM11	COM11	COM11
COM12	COM12	COM12	COM12	COM12	COM12	COM12	COM12	COM12
COM13	COM13	COM13	COM13	COM13	COM13	COM13	COM13	COM13
COM14	COM14	COM14	COM14	COM14	COM14	COM14	COM14	COM14
COM15	COM15	COM15	COM15	COM15	COM15	COM15	COM15	COM15
COM16	COM16	COM16	COM16	COM16	COM16	COM16	COM16	NON-SELECT*
COM17	COM17	COM17	COM17	COM17	COM17	COM17	COM17	NON-SELECT*
COM18	COM18	COM18	COM18	COM18	COM18	COM18	COM18	NON-SELECT*
COM19	COM19	COM19	COM19	COM19	COM19	COM19	COM19	NON-SELECT*
COM20	COM20	COM20	COM20	COM20	COM20	COM20	COM20	NON-SELECT*
COM21	COM21	COM21	COM21	COM21	COM21	COM21	COM21	NON-SELECT*
COM22	COM22	COM22	COM22	COM22	COM22	COM22	COM22	NON-SELECT*
COM23	COM23	COM23	COM23	COM23	COM23	COM23	COM23	NON-SELECT*
COM24	COM24	COM24	COM24	COM24	COM24	COM24	COM24	NON-SELECT*
COM25	COM25	COM25	COM25	COM25	COM25	COM25	COM25	NON-SELECT*
COM26	COM26	COM26	COM26	COM26	COM26	COM26	COM26	NON-SELECT*
COM27	COM27	COM27	COM27	COM27	COM27	COM27	COM27	NON-SELECT*
COM28	COM28	COM28	COM28	COM28	COM28	COM28	COM28	NON-SELECT*
COM29	COM29	COM29	COM29	COM29	COM29	COM29	COM29	NON-SELECT*
COM30	COM30	COM30	COM30	COM30	COM30	COM30	COM30	NON-SELECT*
COM31	COM31	COM31	COM31	COM31	COM31	COM31	COM31	NON-SELECT*
COM32	COM32	COM32	COM32	COM32	COM32	COM32	NON-SELECT*	NON-SELECT*
COM33	COM33	COM33	COM33	COM33	COM33	NON-SELECT*	NON-SELECT*	NON-SELECT*
COM34	COM34	COM34	COM34	COM34	COM34	NON-SELECT*	NON-SELECT*	NON-SELECT*
COM35	COM35	COM35	COM35	COM35	COM35	NON-SELECT*	NON-SELECT*	NON-SELECT*
COM36	COM36	COM36	COM36	COM36	COM36	NON-SELECT*	NON-SELECT*	NON-SELECT*
COM37	COM37	COM37	COM37	COM37	COM37	NON-SELECT*	NON-SELECT*	NON-SELECT*
COM38	COM38	COM38	COM38	COM38	COM38	NON-SELECT*	NON-SELECT*	NON-SELECT*
COM39	COM39	COM39	COM39	COM39	COM39	NON-SELECT*	NON-SELECT*	NON-SELECT*
COM40	COM40	COM40	COM40	COM40	COM40	NON-SELECT*	NON-SELECT*	NON-SELECT*
COM41	COM41	COM41	COM41	COM41	COM41	NON-SELECT*	NON-SELECT*	NON-SELECT*
COM42	COM42	COM42	COM42	COM42	COM42	NON-SELECT*	NON-SELECT*	NON-SELECT*
COM43	COM43	COM43	COM43	COM43	COM43	NON-SELECT*	NON-SELECT*	NON-SELECT*
COM44	COM44	COM44	COM44	COM44	COM44	NON-SELECT*	NON-SELECT*	NON-SELECT*
COM45	COM45	COM45	COM45	COM45	COM45	NON-SELECT*	NON-SELECT*	NON-SELECT*
COM46	COM46	COM46	COM46	COM46	COM46	NON-SELECT*	NON-SELECT*	NON-SELECT*
COM47	COM47	COM47	COM47	COM47	COM47	NON-SELECT*	NON-SELECT*	NON-SELECT*
COM48	COM48	COM48	COM48	COM48	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
COM49	COM49	COM49	COM49	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
COM50	COM50	COM50	COM50	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
COM51	COM51	COM51	COM51	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
COM52	COM52	COM52	COM52	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
COM53	COM53	COM53	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
COM54	COM54	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
COM55	COM55	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
COM56	COM56	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
COM57	COM57	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
COM58	COM58	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
COM59	COM59	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
COM60	COM60	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
COM61	COM61	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
COM62	COM62	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
COM63	COM63	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*

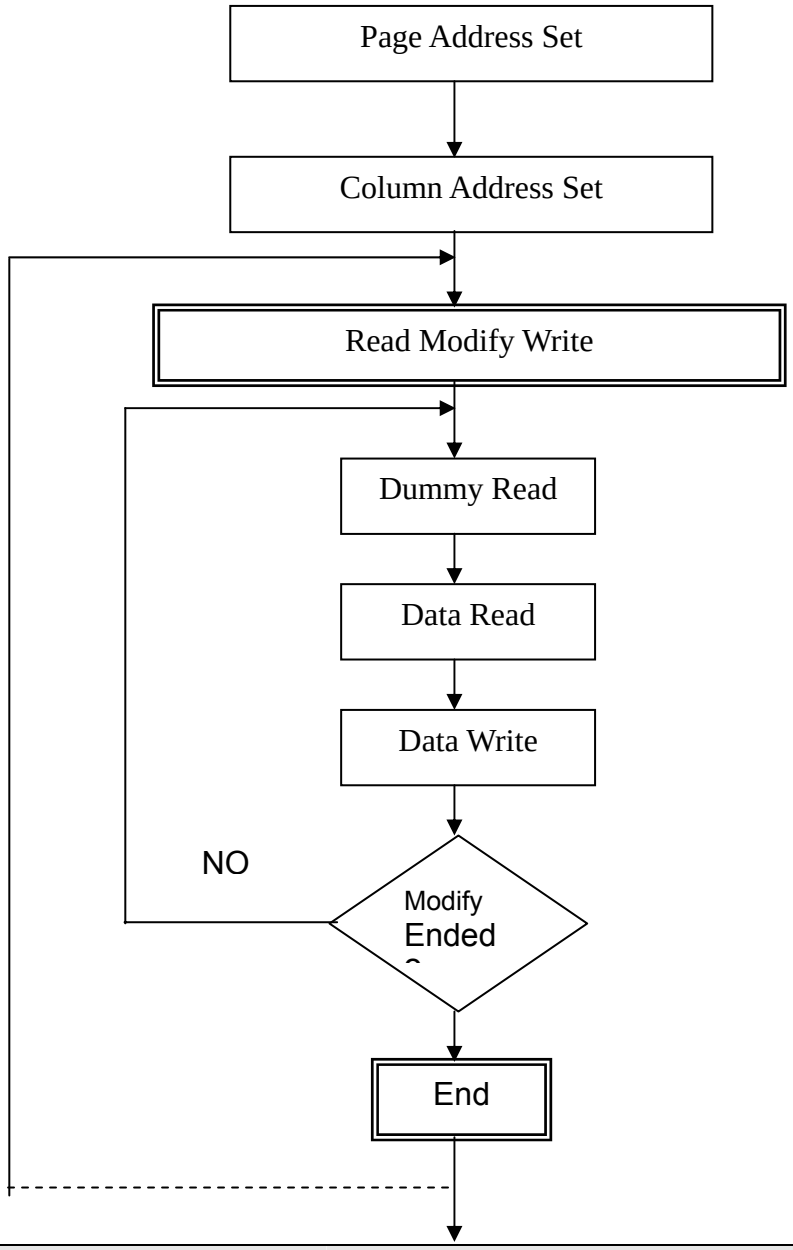
Note：

*The COM will output a Non-Select COM signal.

END TIMING

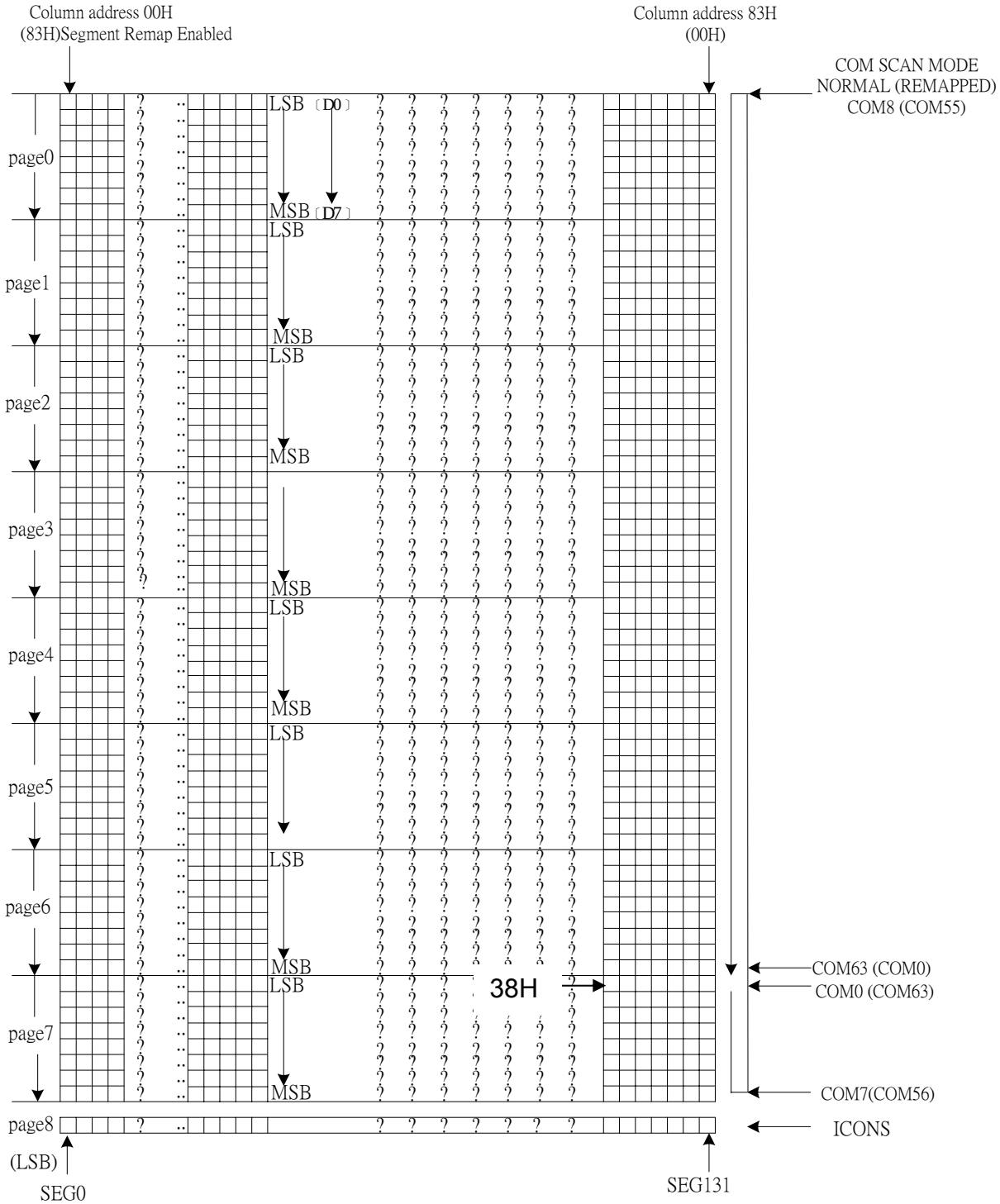


CURSOR BLINKING SEQUENCE



GRAPHIC DISPLAY DATA RAM

(GDDRAM) address map with display start line set to 38h.



Note: The configuration in parentheses represent the remapping of Rows and Columns

ABSOLUTE MAXIMUM RATING

(Unless otherwise stated, Ta=25℃)

Parameter	Symbol	Min	Max.	Unit
Supply Voltage	V_{16}	-0.3	+18	V
	V_{DD}	-0.3	+5.5	V
I/O Pin Voltage	V_X	-0.3	V_{DD}+0.3	V
Operating Temperature	t_{OPR}	-40	+85	℃
Storage Temperature	t_{STG}	-65	+150	℃

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description.

AC CHARACTERISTICS

AC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD}=2.4 to 3.5V, T_A=25℃)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC}	Oscillation Frequency of Display Timing	V_{DD}=2.7V, I_{BVR}=8uA	35	40	42	kHz
F_{FRM}	Frame Frequency for 65 MUX Mode	132×64 Graphic Display Mode, Display ON, Internal Oscillator Enabled		$\frac{F_{OSC}}{6 \times 65}$		Hz
		132×64 Graphic Display Mode, Display ON, Internal Oscillator Disabled, External clock with freq., Fext (Fext=Fosc/6), feeding to CL pin.		$\frac{F_{ext}}{6 \times 65}$		Hz

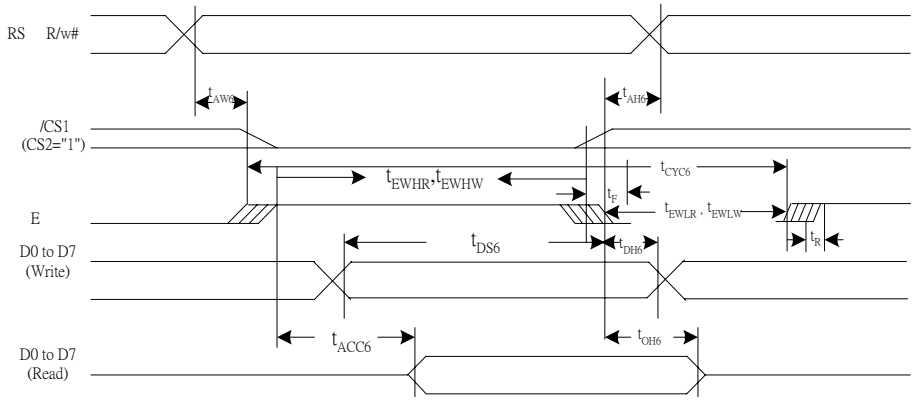
DC CHARACTERISTICS

DC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD}=2.4 to 3.5V, T_A=25℃)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{16}	Operating Voltage		7	-	16	V
V_{DD}	Logic Supply Voltage		2.4	2.7	5.5	V
V_{OH}	HIGH Logic Output Level	Iout=100uA, 3.3MHz	0.9* V_{DD}	-	V_{DD}	V
V_{OL}	LOW Logic Output Level	Iout=100uA, 3.3MHz	0	-	0.1* V_{DD}	V
V_{IH}	HIGH Logic Input Level	Iout=100uA, 3.3MHz	0.8* V_{DD}	-	V_{DD}	V
V_{IL}	LOW Logic Input Level	Iout=100uA, 3.3MHz	0	-	0.2* V_{DD}	V
I_{SLEEP}	Sleep mode Current	V_{DD}=2.7V, I_{BVR}=8uA, No Panel attached	-	0.2	5	μA
I_{16}	V_{16} Supply Current V_{DD}=2.7V, V_{16}=9V, I_{BVR}=8uA, max Frame rate, Brightness=FF, All one pattern, Display on, no loading	Brightness = FF		580	680	μA
		Brightness = AF		480		
I_{DD}	V_{DD} Supply Current V_{DD}=2.7V, V_{16}=9V, I_{BVR}=8uA, max Frame rate, Brightness=FF, All one pattern, Display on, no loading	Brightness = FF	-	600	700	μA
		Brightness = AF		500		μA
I_{SEG}	Normal Bias Current Mode V_{DD}=2.7V, V_{16}=9V, I_{BVR}=8uA, All one pattern, Display on, Segment pin under test is connected with a 20kΩ resistive load to V_{SS}	Brightness = F	330	370	410	μA
		Brightness = AF	215	240	265	
		Brightness = 5F	100	130	145	
		Brightness = 0F	0	20	40	
	LOW Bias Current Mode V_{DD}=2.7V, V_{16}=9V, I_{BVR}=8uA, All one pattern, Display on, Segment pin under test is connected with a 20kΩ resistive load to V_{SS}	Brightness = FF	180	210	240	μA
		Brightness = AF	110	130	160	
		Brightness = 5F	55	75	95	
		Brightness = 0F	0	15	30	
Dev	Segment output current uniformity	Dev=(I_{SEG}-I_{MID})/I_{MID} I_{MID}=(I_{MAX}+I_{MIN})/2 I_{SEG}〔0:131〕=Segment current at Brightness=FF	-	-	±5	%
Adj Dev	Adjacent pin output current uniformity (Brightness=FF)	Adj Dev=(I〔n〕-I〔n+1〕)/(I〔n〕+I〔n+1〕)	-	±4.0	-	%
R_{ON-C}	Common Output On Resistance	V_{16}-V_{SS}=11.7V Iout=30mA;	-	30	40	Ω

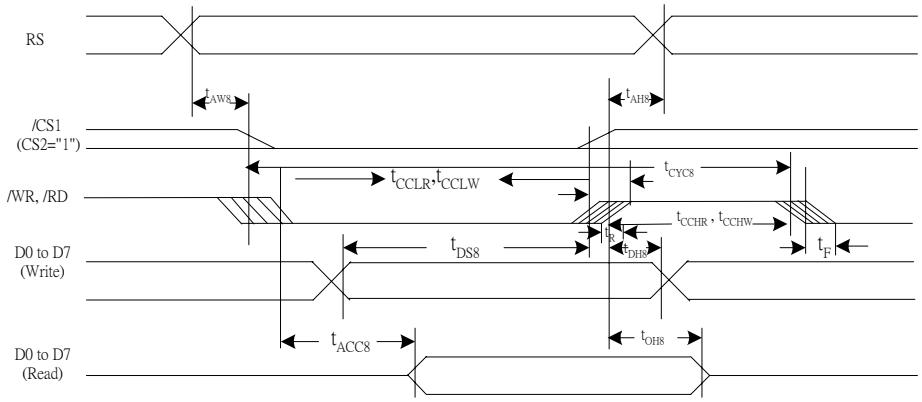
TIMING CHARACTERISTICS

READ/WRITE CHARACTERISTICS FOR 6800 SERIES MPU



Item		Signal	Symbol	Condition	Rating		Units
					Min	Max	
Address hold time		RS, /CS1	t_{AH6}		10	—	ns
Address setup time			t_{AW6}		20	—	ns
System cycle time		/CS1	t_{CYC6}		300	—	ns
Data setup time		D0 to D7	t_{DS6}		40	—	ns
Data hold time			t_{DH6}		15	—	ns
Access time			t_{ACC6}	C_L=100pF	—	140	ns
Output disable time			t_{OH6}		—	70	ns
Enable H pulse time	Read	E	t_{EWHR}		120	—	ns
	Write		t_{EWHW}		60	—	ns
Enable L pulse time	Read	E	t_{EWLR}		120	—	ns
	Write		t_{EWLW}		60	—	ns
Rise Time			t_R		—	15	ns
Fall Time			t_F		—	15	ns

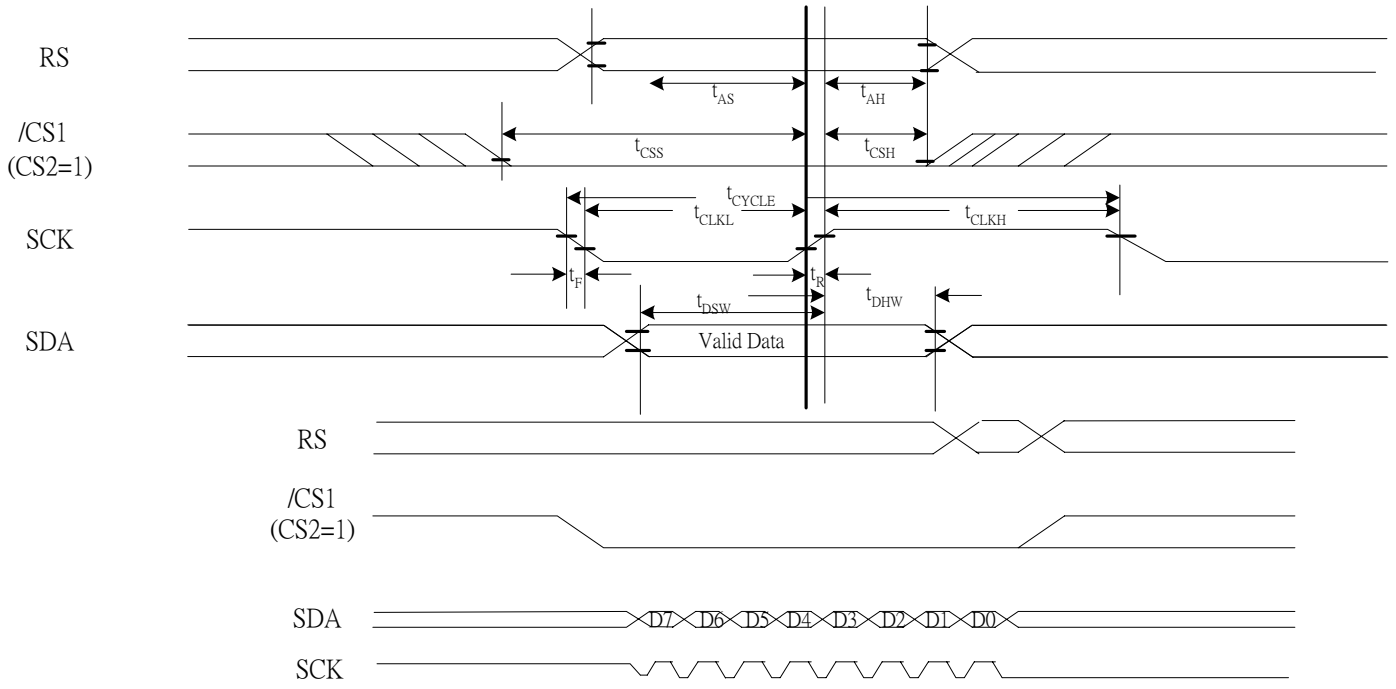
Read/Write Characteristics for the 8080 Series MPU



Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Address hold time	RS	t_{AH8}		10	—	ns
Address setup time		t_{AW8}		20	—	ns
System cycle time	RS	t_{CYC8}		300	—	ns
Control L pulse width (/WR)	/WR	t_{CCLW}		60	—	ns
Control L pulse width (/RD)	/RD	t_{CCLR}		120	—	ns
Control H pulse width (/WR)	/WR	t_{CCHW}		60	—	ns
Control H pulse width (/RD)	/RD	t_{CCHR}		120	—	ns
Data setup time	D0 to D7	t_{DS8}		40	—	ns
Address hold time		t_{DH8}		15	—	ns
$\overline{RD}$ access time		t_{ACC8}	C_L=100pF	—	140	ns
Output disable time		t_{OH8}		—	70	ns
Rise Time		t_R		—	15	ns
Fall Time		t_F		—	15	ns

SERIAL PERIPHERAL INTERFACE CHARACTERISTICS

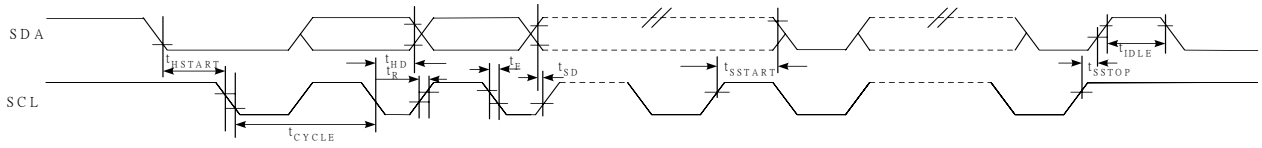
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock LOW Time	100	-	-	ns
t_{CLKH}	Clock HIGH Time	100	-	-	ns
t_R	Rise Time	–	-	15	ns
t_F	Fall Time	-	-	15	ns



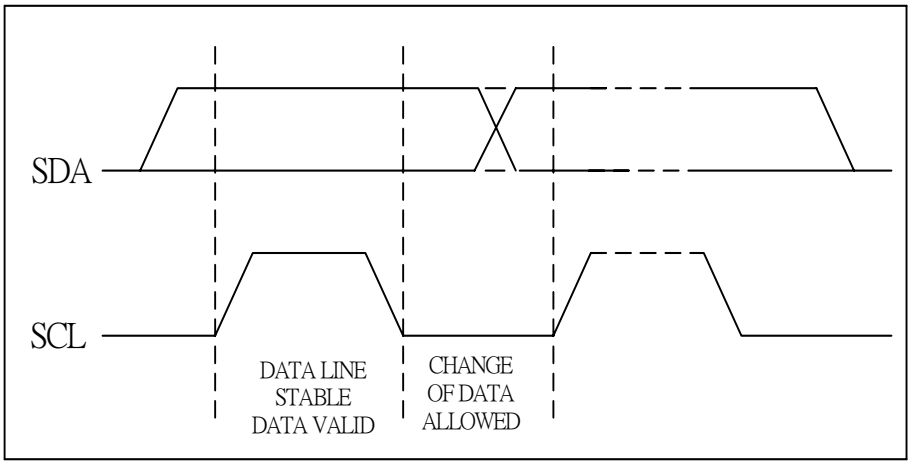
Serial Peripheral Interface Characteristics

I²C INTERFACE TIMING CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	µs
t_{HD}	Data Hold Time	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	µs
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	µs
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	µs



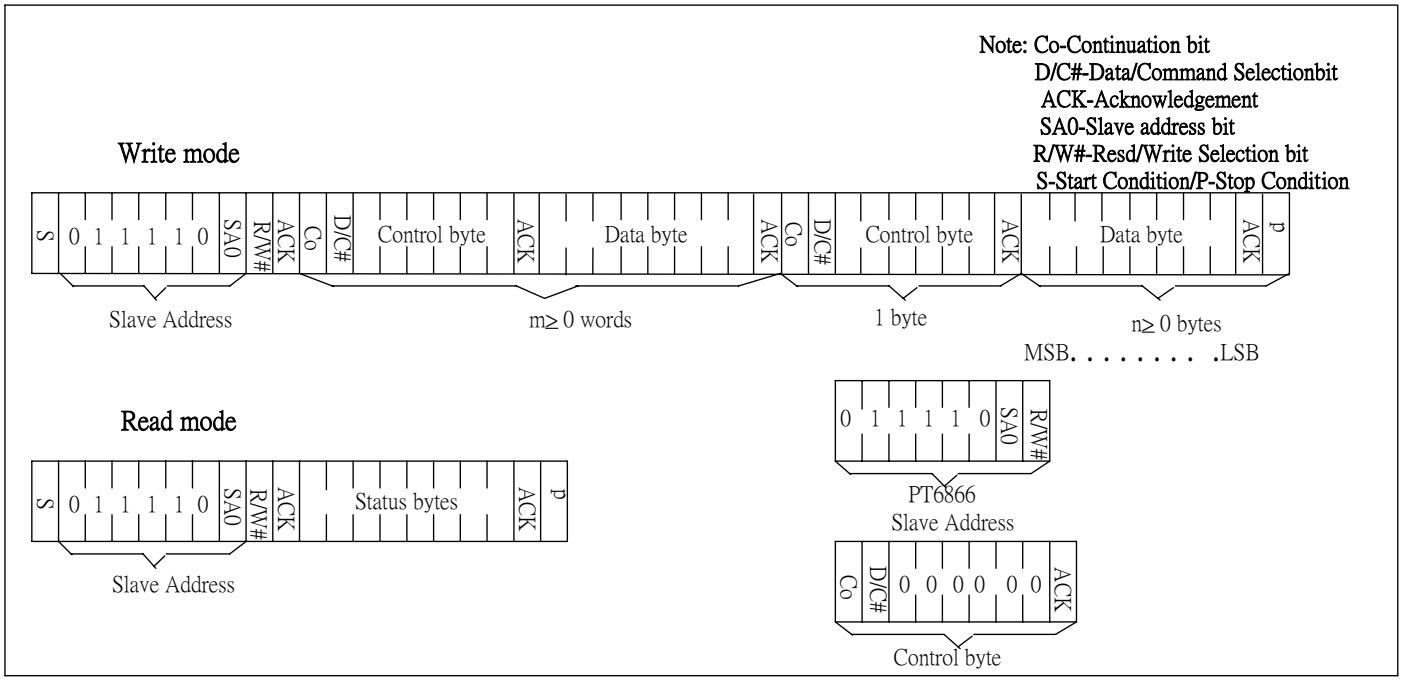
I²C Interface Timing Characteristics



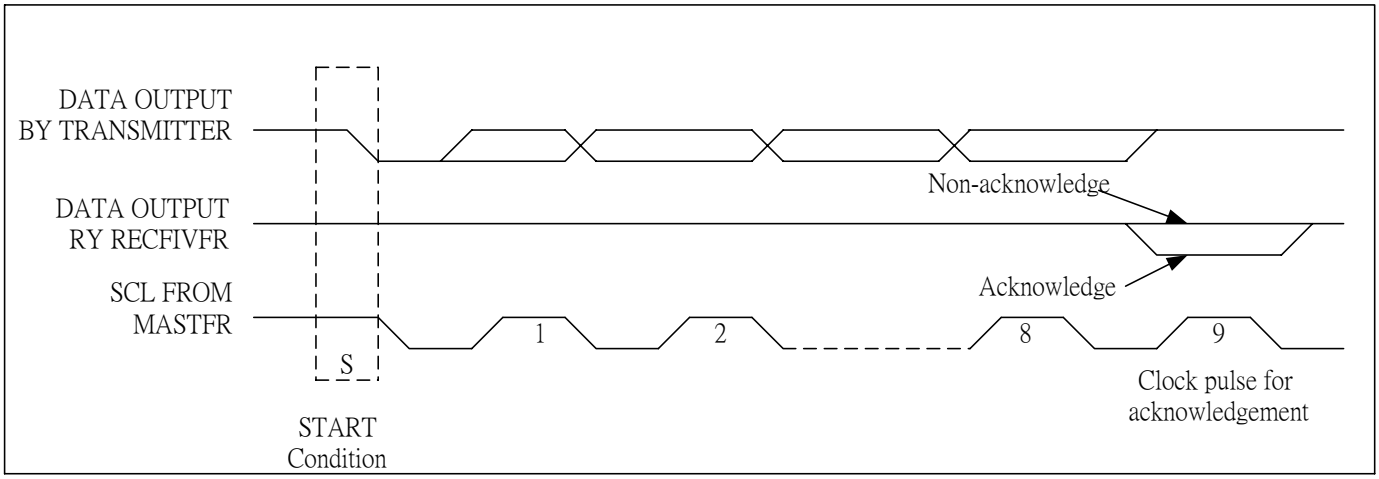
Bit transfer on I²C-bus

I²C-BUS WRITE DATA AND READ REGISTER STATUS

The I²C-bus interface gives access to write data and command into the device. Please refer to the below for the write/Read mode of I²C-bus in chronological order.



I²C BUS DATA FORMAT



Definition of the acknowledgement condition

Write mode

1. The master device initiates the data communication by a start condition. The definition of the start condition is shown in I^2C Interface Timing Characteristics. The start condition is established by pulling the SDA from high to low while the SCL stays high.
2. The slave address is following the start condition for recognition use. For the PT6866, the slave address if either “b0111101” (for master device) or “b0111100” (for slave device) by changing the SA0 to high or low.
3. The write mode is established by setting the R/W# bit to logic “0”.
4. An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. Please refer to definition of the acknowledgement condition for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the high period of the acknowledgement related clock pulse.
5. After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six “0”s.
   - If the Co bit is set as logic “0”, the transmission of the following information will contain data bytes only.
   - The D/C# bit determines the next data byte is acted as a command or a data. If the D/C# bit is set

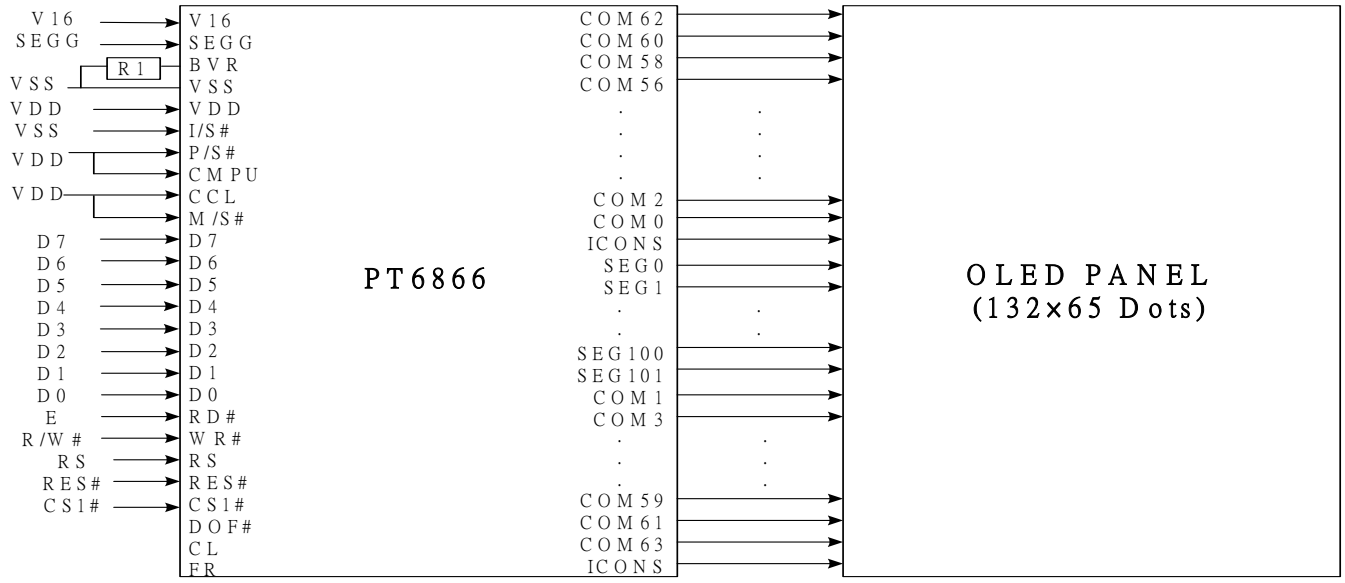
   to logic “0”, it defines the following data byte as a command. If the D/C# bit is set to logic “1”, it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.
6. Acknowledge bit will be generated after receiving each byte.
7. The write mode will be finished when a stop condition is applied. The stop condition is also defined in I^2C Interface Timing Characteristics. The stop condition is established by pulling the “SDA in” from low to high while the “SCL” stays high.

Read mode (Read status register)

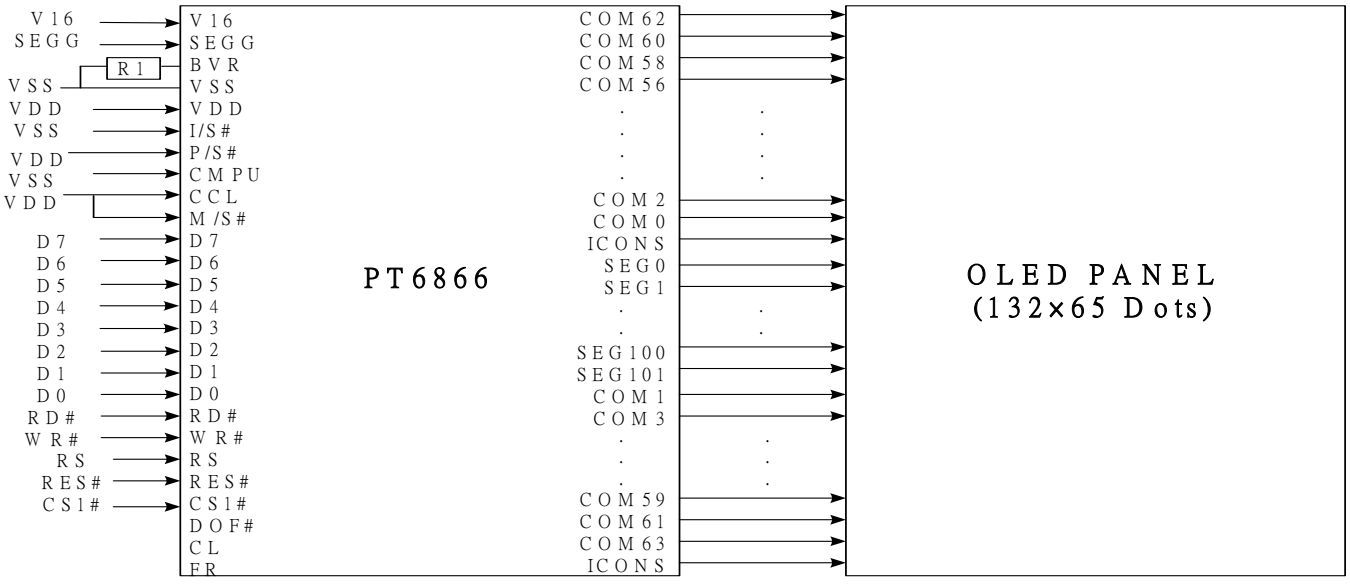
1. The master device firstly initiates the data communication by a start condition. The definition of the start condition is shown in I2C Interface Timing Characteristics.
2. The slave address is following the start condition for recognition use. For the PT6866, the slave address is either “b0111101” (for master device) or “b0111100” (for slave device).
3. The read mode is established by setting R/W# bit to logic “1”. The read mode allows the MCU to monitor the internal status of the chip.
4. An acknowledgement signal will be generated after sending one byte of data, including the slave address and the R/W# bit. Please refer to the definition of the acknowledgement condition for the graphical representation of the acknowledge signal.
5. The status of the register will be read at the next status byte. Please refer to the Command Table for the explanation of the status byte.
6. The read mode will be finished when a stop condition is applied. The stop condition which is sent from MCU is also defined in I2C Interface Timing Characteristics.

APPLICATION EXAMPLE

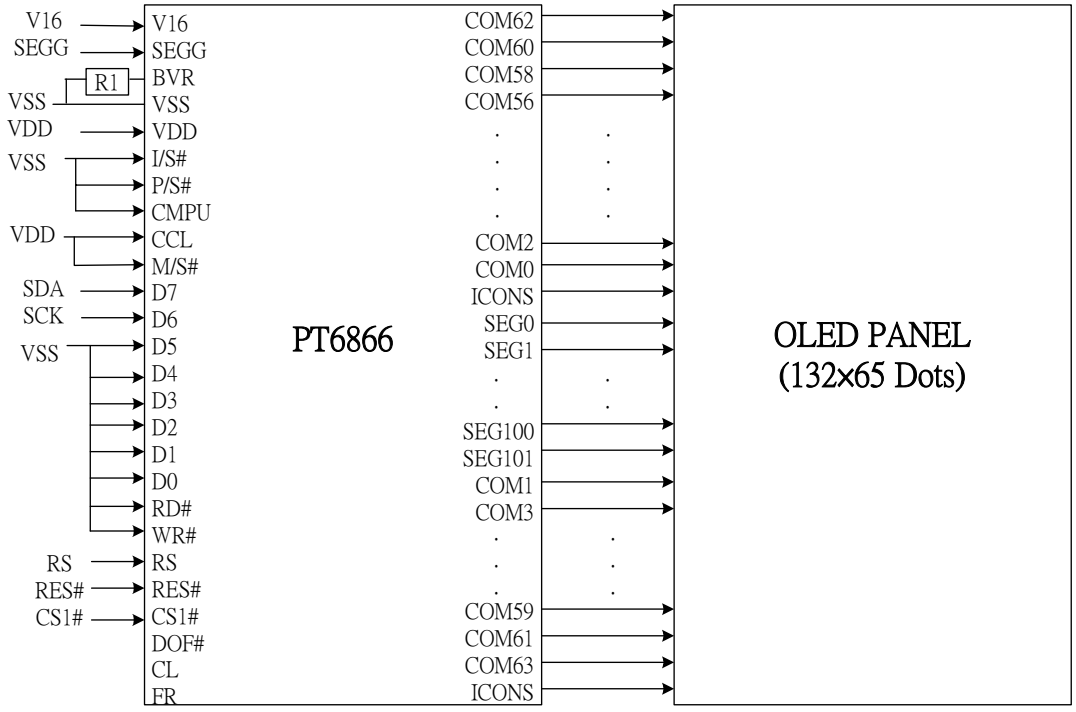
6800 Series Interface



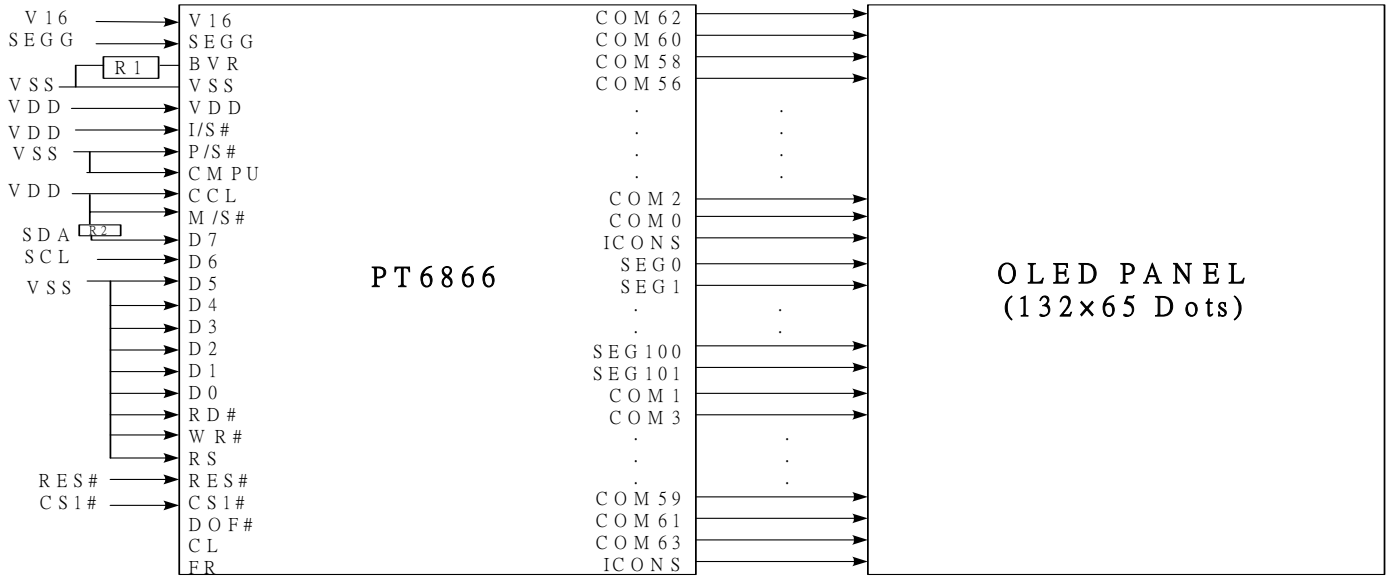
8080 Series Interface



Serial Peripheral Interface



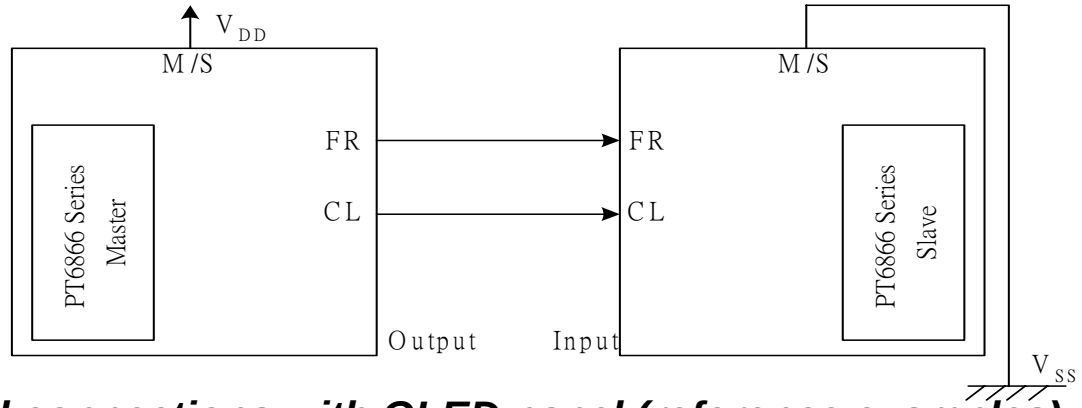
I²c Interface



Note: 1.Connection refer to PIN DESCRITION
2.R1=130KΩ, R2=10KΩ

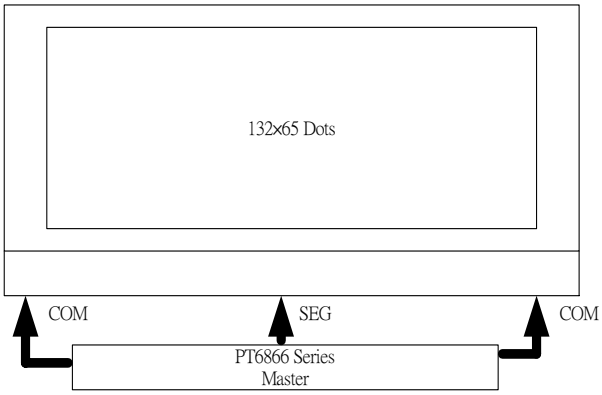
CONNECTIONS BETWEEN OLED DRIVERS (REFERENCE EXAMPLE)

The OLED display area can be enlarged with ease through the use of multiple PT6866 Series chips. Use a same equipment type.

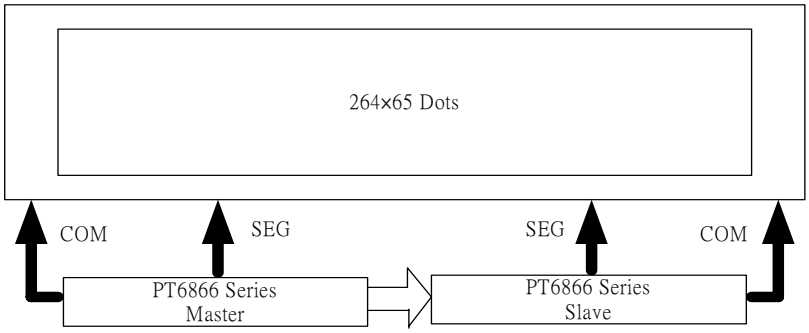


Typical connections with OLED panel (reference examples)

(1)Single-chip Structure

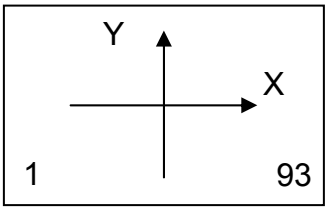


(2)Double-chip Structure



PAD COORDINATES (COORDINATE UNIT: MM)

Pad NO.	PT6866 Pad Name	X-pos	Y-pos
1	VDD	-4691.4	-833.2
2	V16	-4578.4	-833.2
3	SEGG	-4465.4	-833.2
4	VSS	-4352.4	-833.2
5	VDD	-4239.4	-833.2
6	FR	-4126.4	-833.2
7	CL	-4013.4	-833.2
8	DOF#	-3900.4	-833.2
9	VSS	-3787.4	-833.2
10	CS1#	-3674.4	-833.2
11	CS2	-3561.4	-833.2
12	VDD	-3448.4	-833.2
13	RES#	-3335.4	-833.2
14	RS	-3222.4	-833.2
15	VSS	-3109.4	-833.2
16	R/W#(WR#)	-2996.4	-833.2
17	E(RD#)	-2883.4	-833.2
18	VDD	-2770.4	-833.2
19	D0	-2657.4	-833.2
20	D1	-2544.4	-833.2
21	D2	-2431.4	-833.2
22	D3	-2318.4	-833.2
23	D4	-2205.4	-833.2
24	D5	-2092.4	-833.2
25	D6	-1979.4	-833.2
26	D7	-1866.4	-833.2
27	VDD	-1753.4	-833.2
28	M/S#	-1640.4	-833.2
29	CCL	-1527.4	-833.2
30	VSS	-1414.4	-833.2
31	CMPU	-1301.4	-833.2
32	P/S#	-1188.4	-833.2
33	VDD	-1075.4	-833.2
34	I/S#	-962.4	-833.2
35	VDD	-849.4	-833.2
36	VSS	-736.4	-833.2
37	V16	-621.5	-833.2
38	VSS	-441.9	-833.2
39	VSS	-349.7	-833.2
40	VSS	-257.5	-833.2
41	VSS	-165.3	-833.2
42	VSS	-73.1	-833.2
43	VSS	19.1	-833.2
44	VSS	111.3	-833.2
45	VSS	203.5	-833.2
46	VSS	295.7	-833.2
47	VSS	387.9	-833.2
48	VSS	480.1	-833.2
49	VSS	572.3	-833.2
50	VSS	664.5	-833.2
51	VSS	756.7	-833.2
52	VSS	848.9	-833.2
53	VSS	941.1	-833.2
54	VSS	1033.3	-833.2
55	VSS	1125.5	-833.2
56	VSS	1217.7	-833.2
57	VSS	1309.9	-833.2
58	VSS	1402.1	-833.2
59	VSS	1494.3	-833.2
60	VSS	1586.5	-833.2
61	VSS	1678.7	-833.2
62	VSS	1770.9	-833.2
63	VSS	1863.1	-833.2
64	VSS	1955.3	-833.2
65	VSS	2047.5	-833.2
66	VSS	2139.7	-833.2
67	VSS	2231.9	-833.2
68	VSS	2324.1	-833.2
69	VSS	2416.3	-833.2
70	VSS	2508.5	-833.2
71	VSS	2600.7	-833.2
72	V16	2782.2	-833.2
73	V16	2895.2	-833.2
74	V16	3008.2	-833.2
75	VDD	3121.2	-833.2
76	VDD	3234.2	-833.2
77	TESTOUT	3347.2	-833.2
78	VSS	3460.2	-833.2
79	VSS	3573.2	-833.2
80	BVR	3686.2	-833.2
81	SEGG	3799.2	-833.2
82	VSS	3912.2	-833.2
83	VSS	4025.2	-833.2
84	VSS	4138.2	-833.2
85	VDD	4251.2	-833.2
86	VDD	4364.2	-833.2
87	VDD	4477.2	-833.2
88	V16	4590.2	-833.2
89	VDD	4703.2	-833.2
90	DUMMY	5542.9	-833.2
91	DUMMY	5629.1	-833.2
92	DUMMY	5629.7	-685
93	DUMMY	5629.7	-625
94	VSS	5629.7	-565
95	COM62	5629.7	-505
96	COM60	5629.7	-445
97	COM58	5629.7	-385
98	COM56	5629.7	-325
99	COM54	5629.7	-265
100	COM52	5629.7	-205
101	COM50	5629.7	-145
102	COM48	5629.7	-85
103	COM46	5629.7	-25
104	COM44	5629.7	35
105	DUMMY	5629.1	95
106	DUMMY	5629.7	155
107	DUMMY	5629.7	215
108	DUMMY	5629.7	275
109	DUMMY	5629.7	335
110	DUMMY	5629.7	395
111	DUMMY	5629.7	455
112	DUMMY	5629.7	515
113	DUMMY	5629.7	575
114	DUMMY	5629.7	635
115	DUMMY	5629.7	695
116	DUMMY	5642.2	912.5
117	DUMMY	5582.2	912.5
118	VSS	5522.2	912.5
119	COM42	5462.2	912.5
120	COM40	5402.2	912.5
121	COM38	5342.2	912.5
122	COM36	5282.2	912.5
123	COM34	5222.2	912.5
124	COM32	5162.2	912.5
125	COM30	5102.2	912.5
126	COM28	5042.2	912.5
127	COM26	4982.2	912.5
128	COM24	4922.2	912.5
129	COM22	4862.2	912.5
130	COM20	4802.2	912.5
131	COM18	4742.2	912.5
132	COM16	4682.2	912.5
133	COM14	4622.2	912.5
134	COM12	4562.2	912.5
135	COM10	4502.2	912.5
136	COM8	4442.2	912.5
137	COM6	4382.2	912.5
138	COM4	4322.2	912.5
139	COM2	4262.2	912.5
140	COM0	4202.2	912.5
141	ICONS	4142.2	912.5
142	SEG0	3990	912.5
143	SEG1	3930	912.5
144	SEG2	3870	912.5
145	SEG3	3810	912.5
146	SEG4	3750	912.5
147	SEG5	3690	912.5
148	SEG6	3630	912.5
149	SEG7	3570	912.5
150	SEG8	3510	912.5
151	SEG9	3450	912.5
152	SEG10	3390	912.5
153	SEG11	3330	912.5
154	SEG12	3270	912.5
155	SEG13	3210	912.5
156	SEG14	3150	912.5
157	SEG15	3090	912.5
158	SEG16	3030	912.5
159	SEG17	2970	912.5
160	SEG18	2910	912.5
161	SEG19	2850	912.5
162	SEG20	2790	912.5
163	SEG21	2730	912.5
164	SEG22	2670	912.5
165	SEG23	2610	912.5
166	V16	2550	912.5
167	SEG24	2490	912.5
168	SEG25	2430	912.5
169	SEG26	2370	912.5
170	SEG27	2310	912.5
171	SEG28	2250	912.5
172	SEG29	2190	912.5
173	SEG30	2130	912.5
174	SEG31	2070	912.5
175	SEG32	2010	912.5
176	SEG33	1950	912.5
177	SEG34	1890	912.5
178	SEG35	1830	912.5
179	SEG36	1770	912.5
180	SEG37	1710	912.5
181	SEG38	1650	912.5
182	SEG39	1590	912.5
183	SEG40	1530	912.5
184	SEG41	1470	912.5
185	SEG42	1410	912.5
186	SEG43	1350	912.5
187	SEG44	1290	912.5
188	SEG45	1230	912.5
189	SEG46	1170	912.5
190	SEG47	1110	912.5
191	SEG48	1050	912.5
192	SEG49	990	912.5
193	SEG50	930	912.5
194	SEG51	870	912.5
195	SEG52	810	912.5
196	SEG53	750	912.5
197	SEG54	690	912.5
198	SEG55	630	912.5
199	SEG56	570	912.5
200	SEG57	510	912.5
201	SEG58	450	912.5
202	SEG59	390	912.5
203	SEG60	330	912.5
204	SEG61	270	912.5
205	SEG62	310	912.5
206	SEG63	150	912.5
207	SEG64	90	912.5
208	SEG65	30	912.5
209	SEG66	-30	912.5
210	SEG67	-90	912.5
211	SEG68	-150	912.5
212	SEG69	-210	912.5
213	SEG70	-270	912.5
214	SEG71	-330	912.5
215	SEG72	-390	912.5
216	SEG73	-450	912.5
217	SEG74	-510	912.5
218	SEG75	-570	912.5
219	SEG76	-630	912.5
220	SEG77	-690	912.5
221	SEG78	-750	912.5
222	SEG79	-810	912.5
223	SEG80	-8710	912.5
224	SEG81	-930	912.5
225	SEG82	-990	912.5
226	SEG83	-1050	912.5
227	SEG84	-1110	912.5
228	SEG85	-1170	912.5
229	V16	-1230	912.5
230	SEG86	-1290	912.5
231	SEG87	-1350	912.5
232	SEG88	-1410	912.5
233	SEG89	-1470	912.5
234	SEG90	-1530	912.5
235	SEG91	-1590	912.5
236	SEG92	-1650	912.5
237	SEG93	-1710	912.5
238	SEG94	-1770	912.5
239	SEG95	-1830	912.5
240	SEG96	-1890	912.5
241	SEG97	-1950	912.5
242	SEG98	-2010	912.5
243	SEG99	-2070	912.5
244	SEG100	-2130	912.5
245	SEG101	-2190	912.5
246	SEG102	-2250	912.5
247	SEG103	-2310	912.5
248	SEG104	-2370	912.5
249	SEG105	-2430	912.5
250	SEG106	-2490	912.5
251	SEG107	-2550	912.5
252	SEG108	-2610	912.5
253	SEG109	-2670	912.5
254	SEG110	-2730	912.5
255	SEG111	-2790	912.5
256	SEG112	-2850	912.5
257	SEG113	-2910	912.5
258	SEG114	-2970	912.5
259	SEG115	-3030	912.5
260	SEG116	-3090	912.5
261	SEG117	-3150	912.5
262	SEG118	-3210	912.5
263	SEG119	-3270	912.5
264	SEG120	-3330	912.5
265	SEG121	-3390	912.5
266	SEG122	-3450	912.5
267	SEG123	-3510	912.5
268	SEG124	-3570	912.5
269	SEG125	-3630	912.5
270	SEG126	-3690	912.5
271	SEG127	-3750	912.5
272	SEG128	-3810	912.5
273	SEG129	-3870	912.5
274	SEG130	-3930	912.5
275	SEG131	-3990	912.5
276	COM3	-4142.2	912.5
277	COM1	-4202.2	912.5
278	COM5	-4262.2	912.5
279	COM7	-4322.2	912.5
280	COM9	-4382.2	912.5
281	COM11	-4442.2	912.5
282	COM13	-4502.2	912.5
283	COM15	-4562.2	912.5
284	COM17	-4622.2	912.5
285	COM19	-4682.2	912.5
286	COM21	-4742.2	912.5
287	COM23	-4802.2	912.5
288	COM25	-4862.2	912.5
289	COM27	-4922.2	912.5
290	COM29	-4982.2	912.5
291	COM31	-5042.2	912.5
292	COM33	-5102.2	912.5
293	COM35	-5162.2	912.5
294	COM37	-5222.2	912.5
295	COM39	-5282.2	912.5
296	COM41	-5342.2	912.5
297	COM43	-5302.2	912.5
298	COM45	-5462.2	912.5
299	VSS	-5522.2	912.5
300	DUMMY	-5582.2	912.5
301	DUMMY	-5642.2	912.5
302	DUMMY	-5629.7	695
303	DUMMY	-5629.7	635
304	DUMMY	-5629.7	575
305	DUMMY	-5629.7	515
306	DUMMY	-5629.7	455
307	DUMMY	-5629.7	395
308	DUMMY	-5629.7	335
309	DUMMY	-5629.7	275
310	DUMMY	-5629.7	215
311	DUMMY	-5629.7	155
312	DUMMY	-5629.7	95
313	COM47	-5629.7	35
314	COM49	-5629.7	-25
315	COM51	-5629.7	-85
316	COM53	-5629.7	-145
317	COM55	-5629.7	-205
318	COM57	-5629.7	-265
319	COM59	-5629.7	-325
320	COM61	-5629.7	-385
321	COM63	-5629.7	-445
322	ICONS	-5629.7	-505
323	DUMMY	-5629.7	-565
324	DUMMY	-5629.7	-625
325	DUMMY	-5629.7	-685
326	DUMMY	-5629.1	-833.2
327	DUMMY	-5542.9	-833.2



Pad 1,2,3…->92
Gold Bumps face

Bump size:

Pad 1-89: 50um×50um

Pad 118~299: 40um×65um

Pad94~117, 300~327
65um×40um

Die Size: 11376um×1944um
I/O pad pitch:113um
SEG pad pitch:60um
COM pad pitch: 60um
Bump Height: Nominal 18um

Remark：
V16: (This is the most positive voltage supply)
VDD: (Chip power supply)
VSS: (GROUND)
SEGG: (GROUND)

TCP PIN ASSIGNMENT

PIN NO	PIN NAME	PIN NO	PIN NAME	PIN NO	PIN NAME	PIN NO	PIN NAME
1	NC	61	COM7	121	SEG56	181	COM36
2	V16	62	COM5	122	SEG55	182	COM38
3	SEGG	63	COM3	123	SEG54	183	COM40
4	BVR	64	COM1	124	SEG53	184	COM42
5	VSS	65	NC	125	SEG52	185	COM44
6	VDD	66	SEG111	126	SEG51	186	COM46
7	I/S#	67	SEG110	127	SEG50	187	COM48
8	P/S#	68	SEG109	128	SEG49	188	COM50
9	CMPU	69	SEG108	129	SEG48	189	COM52
10	VSS	70	SEG107	130	SEG47	190	COM54
11	CCL	71	SEG106	131	SEG46	191	COM56
12	D7	72	SEG105	132	SEG45	192	COM58
13	D6	73	SEG104	133	SEG44	193	COM60
14	D5	74	SEG103	134	SEG43	194	COM62
15	D4	75	SEG102	135	SEG42	195	NC
16	D3	76	SEG101	136	SEG41		
17	D2	77	SEG100	137	SEG40		
18	D1	78	SEG99	138	SEG39		
19	D0	79	SEG98	139	SEG38		
20	VDD	80	SEG97	140	SEG37		
21	E(RD#)	81	SEG96	141	SEG36		
22	R/W#(WR#)	82	SEG95	142	SEG35		
23	RS	83	SEG94	143	SEG34		
24	RES#	84	SEG93	144	SEG33		
25	CS1#	85	SEG92	145	SEG32		
26	CL	86	SEG91	146	SEG31		
27	VDD	87	SEG90	147	SEG30		
28	VSS	88	SEG89	148	SEG29		
29	SEGG	89	SEG88	149	SEG28		
30	V16	90	SEG87	150	SEG27		
31	NC	91	SEG86	151	SEG26		
32	NC	92	SEG85	152	SEG25		
33	COM63	93	SEG84	153	SEG24		
34	COM61	94	SEG83	154	SEG23		
35	COM59	95	SEG82	155	SEG22		
36	COM57	96	SEG81	156	SEG21		
37	COM55	97	SEG80	157	SEG20		
38	COM53	98	SEG79	158	SEG19		
39	COM51	99	SEG78	159	SEG18		
40	COM49	100	SEG77	160	SEG17		
41	COM47	101	SEG76	161	SEG16		
42	COM45	102	SEG75	162	NC		
43	COM43	103	SEG74	163	COM0		
44	COM41	104	SEG73	164	COM2		
45	COM39	105	SEG72	165	COM4		
46	COM37	106	SEG71	166	COM6		
47	COM35	107	SEG70	167	COM8		
48	COM33	108	SEG69	168	COM10		
49	COM31	109	SEG68	169	COM12		
50	COM29	110	SEG67	170	COM14		
51	COM27	111	SEG66	171	COM16		
52	COM25	112	SEG65	172	COM18		
53	COM23	113	SEG64	173	COM20		
54	COM21	114	SEG63	174	COM22		
55	COM19	115	SEG62	175	COM24		
56	COM17	116	SEG61	176	COM26		
57	COM15	117	SEG60	177	COM28		
58	COM13	118	SEG59	178	COM30		
59	COM11	119	SEG58	179	COM32		
60	COM9	120	SEG57	180	COM34		

LOCATION OF TCP PIN