Product Specification

(Preliminary)

Part Name: OEL Display Module
Part ID: UG-2828GDEAF02
Doc No.: SAS1-D007-A

http://vfdclock.jimdo.com

Customer:
Approved by

From: Univision Technology Inc.
Approved by

Univision Technology Inc.
8, Kebei RD 2, Science Park, Chu-Nan, Taiwan 350, R.O.C.

Notes:

1. Please contact Univision Technology Inc. before assigning your product based on this module specification
2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by Univision Technology Inc. for any intellectual property claims or other problems that may result from application based on the module described herein.

Revised History

Part Number	Revision	Revision Content	Revised on
UG-2828GDEAF02	A	New	Mar 31, 2006

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Contents

1. Basic Specifications

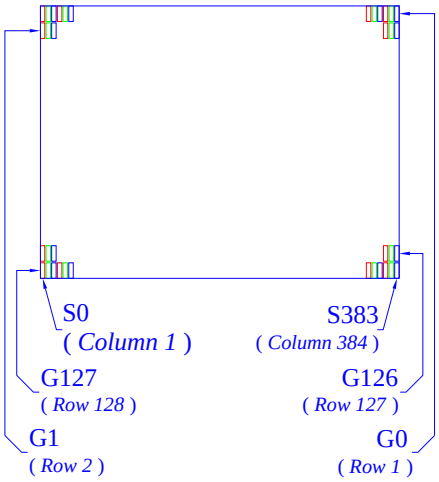
1.1 Display Specifications

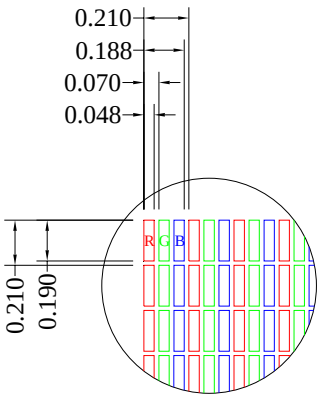
1) Display Mode: Passive Matrix
2) Display Color: 262,144 Colors (Maximum)
3) Drive Duty: 1/128 Duty

1.2 Mechanical Specifications

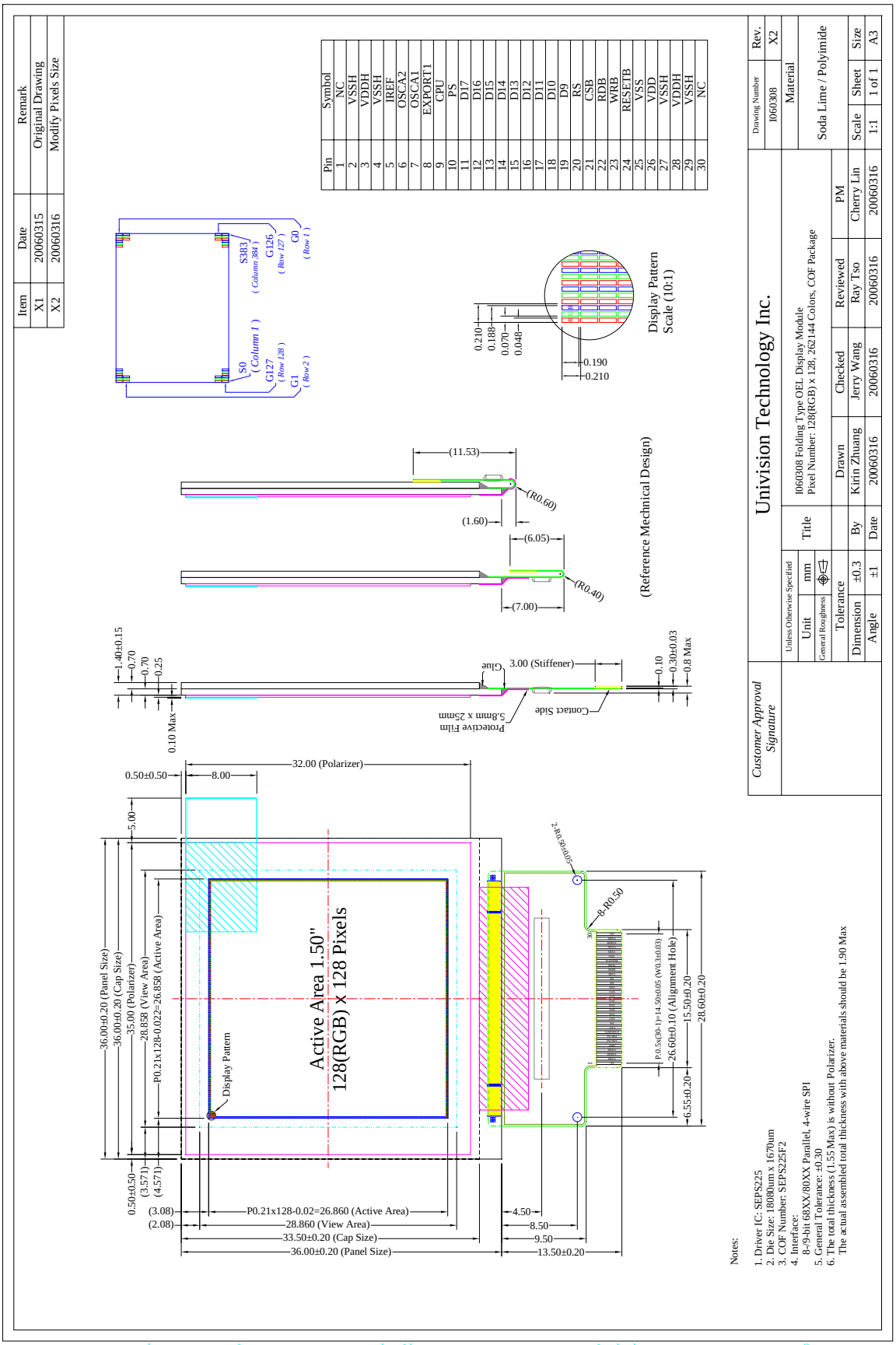
1) Outline Drawing: According to the annexed outline drawing number
2) Number of Pixels: 128(RGB) × 128
3) Panel Size: 36.00 × 36.00 × 1.7 (mm)
4) Active Area: 26.86 × 26.86 (mm)
5) Pixel Pitch: 0.07 × 0.21 (mm)
6) Pixel Size: 0.048 × 0.19 (mm)
7) Weight: 4.35 (g)

1.3 Active Area & Pixel Construction





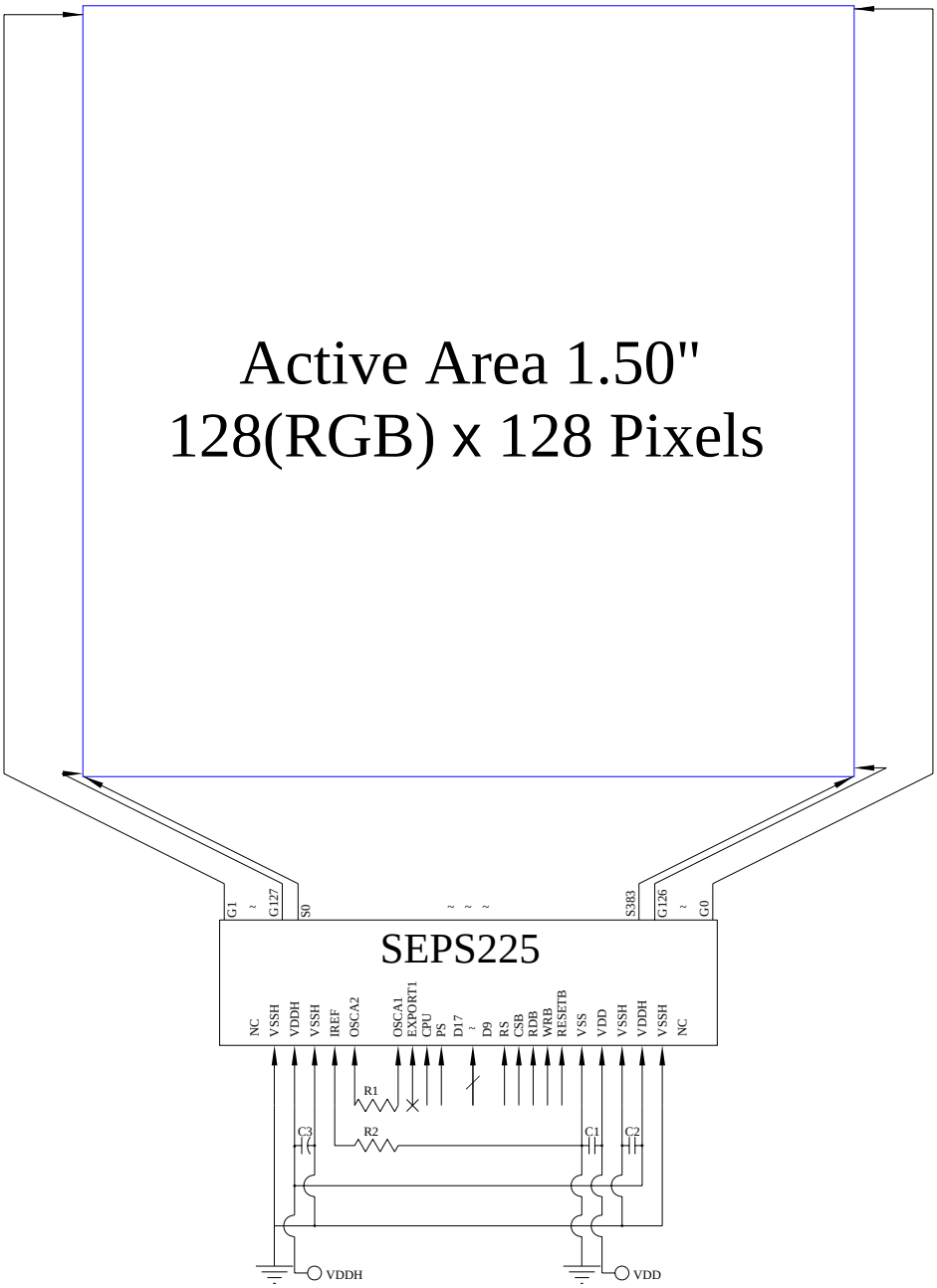
1.4 Mechanical Drawing



1.5 Pin Definition

<table>
<tr><th>Pin Number</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>2,4,27,29</td><td>VSSH</td><td>P</td><td>Return Ground for VDDH</td></tr>
<tr><td>3,28</td><td>VDDH</td><td>P</td><td>External Column Driving Power Supply.</td></tr>
<tr><td>25</td><td>VSS</td><td>P</td><td>Power supply ground</td></tr>
<tr><td>26</td><td>VDD.</td><td>P</td><td>Logic power supply.</td></tr>
<tr><td>5</td><td>IREF</td><td>I/O</td><td>Current Reference for Brightness Adjustment
Tie 70KΩ resistor to VSS.</td></tr>
<tr><td>6</td><td>OSCA2</td><td>O</td><td>Fine adjustment for oscillation
Tie 10 KΩ resistor to OSCA1 between OSCA2.
When the external clock mode is selected, OSCA1 is used external clock input.</td></tr>
<tr><td>7</td><td>OSCA1</td><td>I</td><td></td></tr>
<tr><td>8</td><td>EXPORT1</td><td>O</td><td>OSC Test</td></tr>
<tr><td>9</td><td>CPU</td><td>I</td><td>Selects the CPU type
Low: 80-series CPU, High: 68-Series CPU.</td></tr>
<tr><td>10</td><td>PS</td><td>I</td><td>Selects parallel/Serial interface type
Low: serial, High: parallel.</td></tr>
<tr><td>11~19</td><td>D17~D9</td><td>I/O</td><td>Host Data Input/Output Bus
These pins are 9-bit bi-directional data bus to be connected with MCU data bus.
<table>
<tr><th>PS</th><th>Description</th></tr>
<tr><td>1</td><td>8_bit bus : D[17:10]
9_bit bus : D[17:9]</td></tr>
<tr><td>0</td><td>D[17] SCL : Synchronous clock input
D[16] SDI : Serial data input
D[15] SDO : Serial data output</td></tr>
</table>
Fix unused pins to the VSS level.</td></tr>
<tr><td>20</td><td>RS</td><td>I</td><td>Selects the data/command
Low: command, High: parameter/data</td></tr>
<tr><td>21</td><td>CSB</td><td>I</td><td>Chip Select
Low: SEPS225 is selected and can be accessed.
High: SEPS225 is not selected and cannot be accessed.</td></tr>
<tr><td>22</td><td>RDB</td><td>I</td><td>Read or Read/Write Enable
80-system bus interface: read strobe signal (active low).
68-system bus interface: bus enable strobe (active high).
When serial mode, fix it to VDD or VSS level.</td></tr>
<tr><td>23</td><td>WRB</td><td>I</td><td>Write or Read/Write Select
80-system bus interface: write strobe signal (active low).
68-system bus interface: read/write select.
Low: write, High: read.
When serial mode, fix it to VDD or VSS level.</td></tr>
<tr><td>24</td><td>RESETB</td><td>I</td><td>Chip Reset
Reset SEPS225 (active low)</td></tr>
<tr><td>1,30</td><td>NC</td><td>-</td><td>No Connection</td></tr>
</table>

1.6 Block Diagram



MCU Interface Selection: PS, CPU
Pins connected to MCU interface: D17~D9, RDB, RS, CSB, WRB, and RESB
* EXPORT1would be left float.

C1: 1μF
C2, C3: 4.7μF
R1: 10kΩ
R2: 70kΩ

2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage	VDD	-0.3	4	V	1, 2
Driver Supply Voltage	VDDH	-0.3	19.5	V	1, 2
Operating Temperature	T_{OP}	-20	70	°C	-
Storage Temperature	T_{STG}	-30	80	°C	-

Note 1: All the above voltages are on the basis of "GND = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

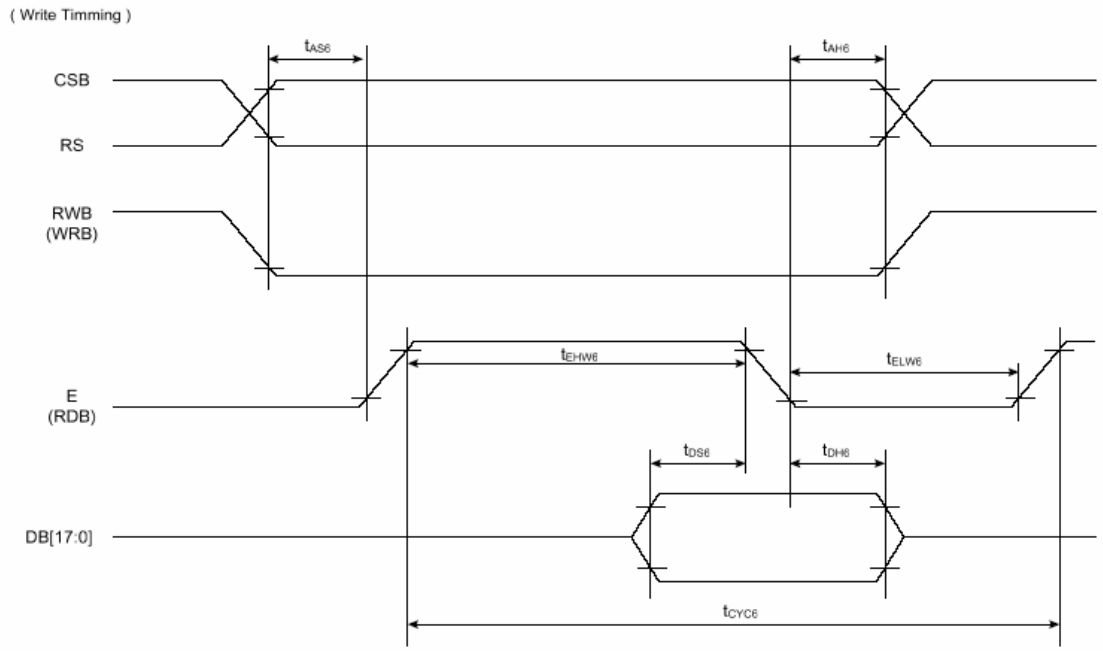
3. Electrical Characteristics

3.1 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	VDD		2.6	2.8	3.3	V
Driver Supply Voltage	VDDH		-	13.0	-	V
High Level Input	V_{IH}		0.8×VDD	-	VDD	V
Low Level Input	V_{IL}		0	-	0.4	V
High Level Output	V_{OH}		VDD-0.4	-	-	V
Low Level Output	V_{OL}		-	-	0.4	V

3.2 AC Characteristics

3.2.1 68XX-Series MPU Parallel Interface Timing Characteristics:

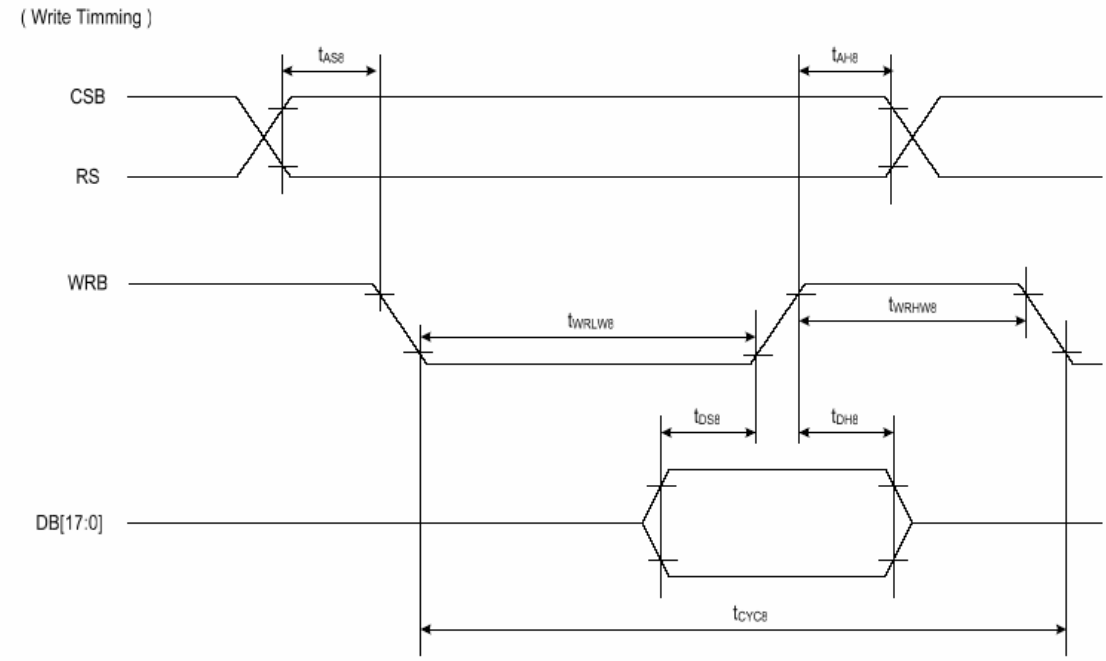


(VDD = 2.8V, Ta = 25℃)

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Address hold timing	t_{AH6}	-	5	-	ns	CSB
Address setup timing	t_{AS6}		5		ns	RS
System cycle timing	t_{CYC6}	-	100	-	ns	E
Write "L" pulse width	t_{ELW6}		45		ns	
Write "H" pulse width	t_{EHW6}		45		ns	
Data setup timing	t_{DS6}	-	40	-	ns	DB[17:0]
Data hold timing	t_{DH6}		10		ns	

notice) All the timing reference is 10% and 90% of VDD.

3.2.2 80XX-Series MPU Parallel Interface Timing Characteristics:

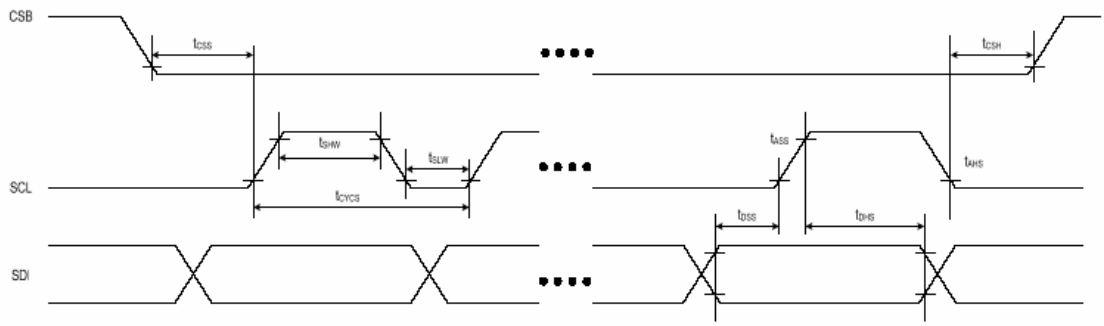


(VDD = 2.8V, Ta = 25℃)

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Address hold timing	t_{AH8}	-	5	-	ns	CSB
Address setup timing	t_{AS8}		5		ns	RS
System cycle timing	t_{CYC8}	-	100	-	ns	WRB
Write "L" pulse width	t_{WRLW8}		45		ns	
Write "H" pulse width	t_{WRHW8}		45		ns	
Data setup timing	t_{DS8}	-	30	-	ns	DB[17:0]
Data hold timing	t_{DH8}		10		ns	

notice) All the timing reference is 10% and 90% of VDD.

3.2.3 Serial Interface Timing Characteristics:



(VDD = 2.8V, Ta = 25℃)

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Serial clock cycle	tCYCS	-	60	-	ns	SCL
SCL "H" pulse width	tSHW		25		ns	
SCL "L" pulse width	tSLW		25		ns	
Data setup timing	tDSS	-	25	-	ns	SDI
Data hold timing	tDHS		25		ns	
CSB-SCL timing	tCSS	-	25	-	ns	CSB
CSB-hold timing	tCSH		25		ns	

notice) All the timing reference is 10% and 90% of VDD.

3.3 Optics & Electrical Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness (White)	L_{br}	Display Average (Note 3)	70	90	-	cd/m^2
C.I.E. (White)	(x) (y)		0.26 0.29	0.30 0.33	0.34 0.37	
C.I.E. (Red)	(x) (y)		0.57 0.32	0.61 0.36	0.65 0.40	
C.I.E. (Green)	(x) (y)		0.26 0.58	0.30 0.62	0.34 0.66	
C.I.E. (Blue)	(x) (y)		0.11 0.13	0.15 0.17	0.19 0.21	
Dark Room Contrast	CR		-	>10000:1	-	
View Angle			>160	-	-	degree

* Optical Measurement Follow the Software Initial Setting with Chapter 4.4 “Initial Code”

3.4 General Electrical Specification

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.6	2.8	3.5	V
Supply Voltage for I/O Pins	V_{DDIO}		1.5	2.8	3.5	V
Driver Supply Voltage	V_{CC}	Note 3	12.5	13.0	13.5	V
Operating Current for V_{DD}	I_{DD}	Note 4	-	2.5	3.5	mA
		Note 5	-	2.5	3.5	mA
Operating Current for V_{CC}	I_{CC}	Note 4	-	20	23	mA
		Note 5	-	30	35	mA

Note 3: Brightness (L_{br}) and Driver Supply Voltage (V_{CC}) are subject to the change of the panel characteristics and the customer’s request.

Note 4: V_{DD} = 2.8V, V_{CC} = 13V, Software Initial Setting follow Chapter 4.4 “Initial Code”, 50% Display Area Turn on.

Note 5: V_{DD} = 2.8V, V_{CC} = 13V, Software Initial Setting follow Chapter 4.4 “Initial Code”, 100% Display Area Turn on.

4. Functional Specification

4.1. Commands

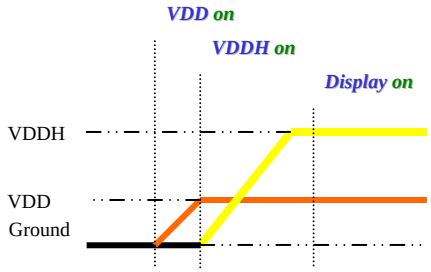
Refer to the Technical Manual for the SEPS225

4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

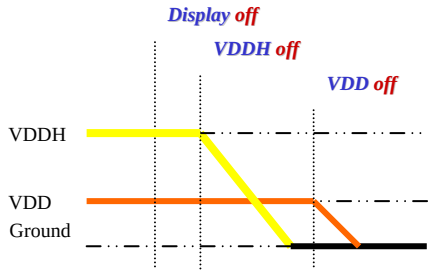
4.2.1 Power up Sequence:

1. Power up VDD
2. Send Display off command
3. Clear Screen
4. Power up VDDH
5. Delay 100ms
   (when VDD is stable)
6. Send Display on command



4.2.2 Power down Sequence:

1. Send Display off command
2. Power down VDDH
3. Delay 100ms
   (when VDDH is reach 0 and panel is completely discharges)
4. Power down VDD



4.3 Reset Circuit

When RESETB input is low, the chip is initialized with the following status:

1. Frame frequency: 90Hz
2. OSC: internal OSC
3. Internal OSC: ON
4. DDRAM write horizontal address: MX1 = 00h, MX2 = 7Fh
5. DDRAM write vertical address: MY1 = 00h, MY2 = 7Fh
6. Display data RAM write: HC = 1, VC = 1, HV = 0
7. RGB data swap: OFF
8. Row scan shift direction: G0, G1, … , G126, G127
9. Column data shift direction: S0, S1, … , S382, S383
10. Display ON/OFF: OFF
11. Panel display size: FX1 = 00h, FX2 = 7Fh, FY1 = 00h, FY2 = 7Fh
12. Display data RAM read column/row address: FAC = 00h, FAR = 00h
13. Precharge time(R/G/B): 0 clock
14. Precharge current(R/G/B): 0 uA
15. Driving current(R/G/B): 0 uA

4.4 Actual Application Example

Initial Code:

```
//OSC control
//EXPORT1 internal clock and OSC operates with external resister
      Write_Register(0x02);
      Write_Parameter(0x01);

//REDUCE_CURRENT
//Reduced driving current : normal
//Power save mode:normal
      Write_Register(0x04);
      Write_Parameter(0x00);

//CLOCK_DIV
//OSC frequency setting : 90Hz
//Display frequency divide ration:1
      Write_Register(0x03);
      Write_Parameter(0x30);

//PRECHARGE_TIME_R
//6 Precharge Time
      Write_Register(0x08);
      Write_Parameter(0x00);

//PRECHARGE_TIME_G
//6 Precharge Time
      Write_Register(0x09);
      Write_Parameter(0x00);

//PRECHARGE_TIME_B
//6 Precharge Time
      Write_Register(0x0A);
      Write_Parameter(0x00);


//PRECHARGE_CURRENT_R
//6 Precharge Time
      Write_Register(0x0B);
      Write_Parameter(0x00);

//PRECHARGE_CURRENT_G
//6 Precharge Time
      Write_Register(0x0C);
      Write_Parameter(0x00);

//PRECHARGE_CURRENT_B
//6 Precharge Time
      Write_Register(0x0D);
      Write_Parameter(0x00);

//DRIVING_CURRENT_R
//128uA
      Write_Register(0x10);
      Write_Parameter(0x4A);

//DRIVING_CURRENT_G
//128uA
      Write_Register(0x11);
```

```
      Write_Parameter(0x4A);

//DRIVING_CURRENT_B
//128uA
      Write_Register(0x12);
      Write_Parameter(0x2F);

//Display mode set
//RGB,column=0→127,column data display control=Normal Dispaly
      Write_Register(0x13);
      Write_Parameter(0x00);

//External interface mode =MPU
      Write_Register(0x14);
      Write_Parameter(0x01);


//MEMORY_WRITE_MODE
//6btis Triple transfer,262K support ,Horizontal address counter is increased,Vertical
address //counter is increased,The data is continuously written horizontally
      Write_Register(0x16);
      Write_Parameter(0x76);

//Memory addrss setting range 0x17~0x19→128x128
      Write_Register(0x17);        //column start
      Write_Parameter(0x00);

      Write_Register(0x18);        //column end
      Write_Parameter(0x7F);

      Write_Register(0x19);        //row start
      Write_Parameter(0x00);

      Write_Register(0x1A);        //row end
       Write_Parameter(0x7F);

//Memory Start Address set   0x20~0x21
      Write_Register(0x20);        // X
      Write_Parameter(0x00);

      Write_Register(0x21);        // Y
       Write_Parameter(0x00);

//DUTY
      Write_Register(0x28);
      Write_Parameter(0x80);//128

  //Display Start LIne
      Write_Register(0x29);
      Write_Parameter(0x00);

//DDRAM Read Address Start point 0x2E~0x2F
      Write_Register(0x2E);        // X
      Write_Parameter(0x00);

      Write_Register(0x2F);        // Y
      Write_Parameter(0x00);

//Display Screen Saver Size 0x33~0x36
      Write_Register(0x33);        //Display Screen Saver Columns Start
```

```
Write_Parameter(0x00);

Write_Register(0x34);        //Display Screen Saver Columns End
Write_Parameter(0x7F);

Write_Register(0x35);        //Display Screen Saver Row Start
Write_Parameter(0x00);

Write_Register(0x36);        //Display Screen Saver Row End
Write_Parameter(0x7F);

Write_Register(0x80);        //IREF→Reference volt. controlled by Exteranl
                             resister
Write_Parameter(0x00);

Write_Register(0x06);        //Display ON
Write_Parameter(0x01);
```

5. Reliability

5.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	70°C, 240 hrs	The operational functions work.
Low Temperature Operation	-20°C, 240 hrs	
High Temperature Storage	80°C, 240 hrs	
Low Temperature Storage	-30°C, 240 hrs	
High Temperature/Humidity Operation	60°C, 90% RH, 120 hrs	
High Temperature/Humidity Storage	60°C, 90% RH, 240 hrs	
Thermal Shock	-40°C ⇔ 85°C, 24 cycles 1 hr dwell	

* The samples used for the above tests do not include polarizer.
* No moisture condensation is observed during tests.

5.2 Lifetime

End of lifetime is specified as 50% of initial brightness.

Parameter	Min	Max	Unit	Condition	Notes
Operating Life Time	10,000	-	Hrs	90 cd/m^2, 50%checkerboard	6
Storage Life Time	20,000	-	Hrs	Ta=25°C, 50%RH	-

Note 6: The average operating lifetime at room temperature is estimated by the accelerated operation at 70°C for 240 hrs.

5.3 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

6. Outgoing Quality Control Specifications

6.1 Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	23 ± 5°C
Humidity:	55 ± 15 %RH
Fluorescent Lamp:	30W
Distance between the Panel & Lamp:	≥ 50 cm
Distance between the Panel & Eyes of the Inspector:	≥ 30 cm

Finger glove (or finger cover) must be worn by the inspector.
Inspection table or jig must be anti-electrostatic.

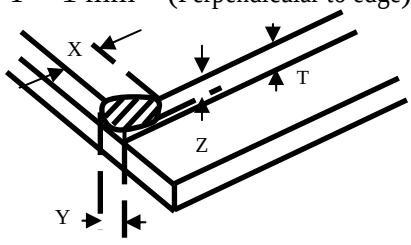
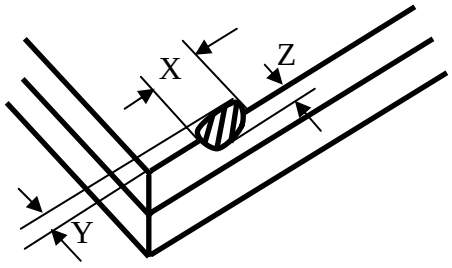
6.2 Sampling Plan

Level II, Normal Inspection, Single Sampling, MIL-STD-105E

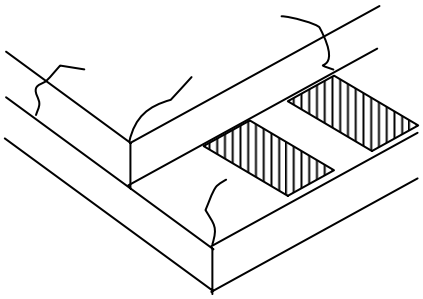
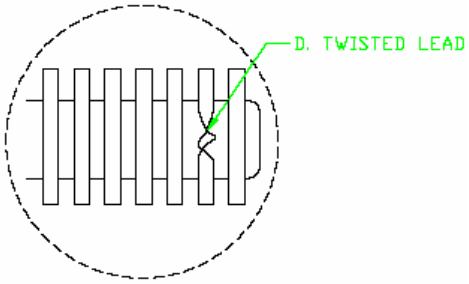
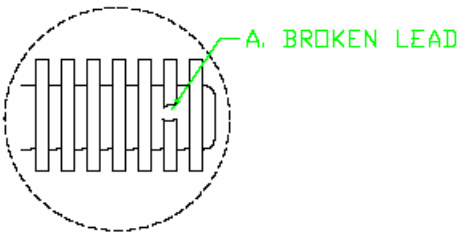
6.3 Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

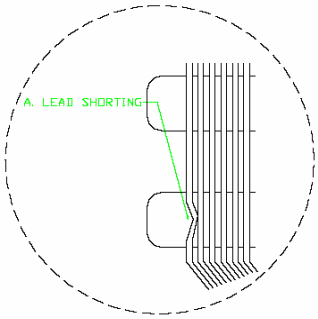
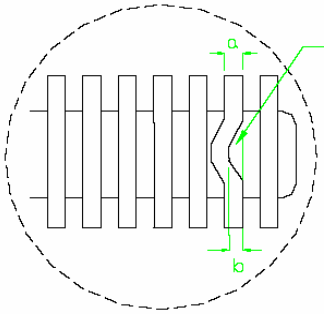
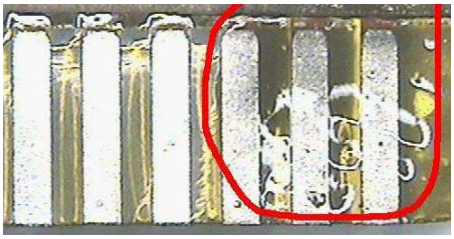
6.3.1 Cosmetic Check (Display Off) in Non-Active Area

Check Item	Classification	Criteria
Panel General Chipping	Minor	X > 6 mm (Along with Edge) Y > 1 mm (Perpendicular to edge)  

6.3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

Check Item	Classification	Criteria
Panel Crack	Minor	Any crack is not allowable. 
Cupper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Terminal Lead Twist	Minor	Not Allowable 
Terminal Lead Broken	Minor	Not Allowable 
Terminal Lead Probe Mark	Acceptable	Ok

6.3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

Check Item	Classification	Criteria
Terminal Lead Bent (Not Twist or Broken)	Minor	NG if any bent lead cause lead shorting. 
	Minor	NG for horizontally bent lead more than 50% of its width. 
Glue or Contamination on Pin (Couldn't Be Removed by Alcohol)	Minor	
Ink Marking on Back Side of panel (Exclude on Film)	Acceptable	Ignore for Any

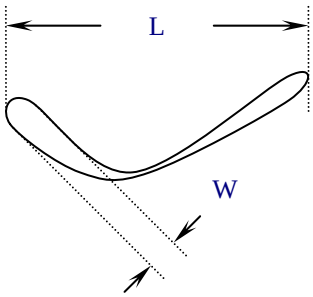
6.3.2 Cosmetic Check (Display Off) in Active Area

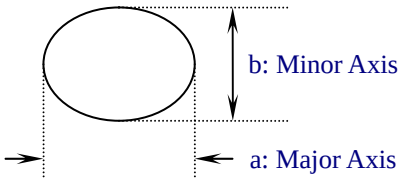
Don't tear off the protective film for only visual check purpose. Otherwise any particle or contamination of air could penetrate & attach onto the surface of polarizer in great probability. It is recommended to execute in clear room environment (class 10k) if actual in necessary.

Check Item	Classification	Criteria	
Any Dirt & Scratch on Protective Film	Acceptable	Ignore for Any	
Scratches, Fiber, Line-Shape Defect ** (On Glass Display Side)	Minor	W ≤ 0.1	Ignore
		W > 0.1, L ≤ 2 L > 2	 n ≤ 1 n = 0
Dirt, Spot-Shape Defect ** (On Glass Display Side)	Minor	Φ ≤ 0.1 0.1 <Φ ≤ 0.25 0.25 <Φ	Ignore n ≤ 1 n = 0
Fingerprint, Flow Mark (On Glass Display Side)	Minor	Not allowable	

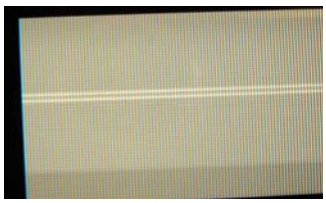
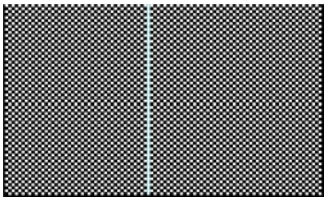
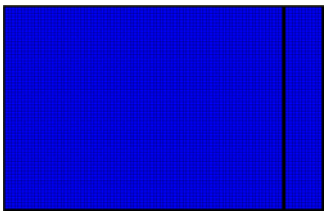
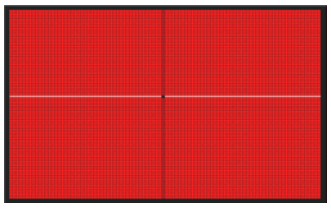
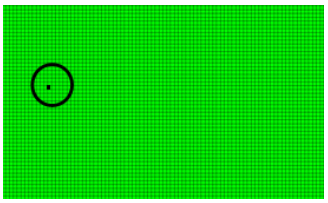
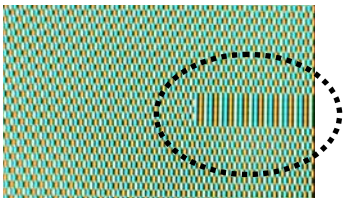
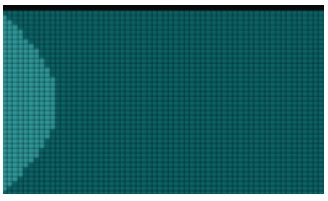
** Distance between any 2 defects should over 10mm

*** Definition of W & L & Φ (unit: mm): Φ = (a + b) / 2

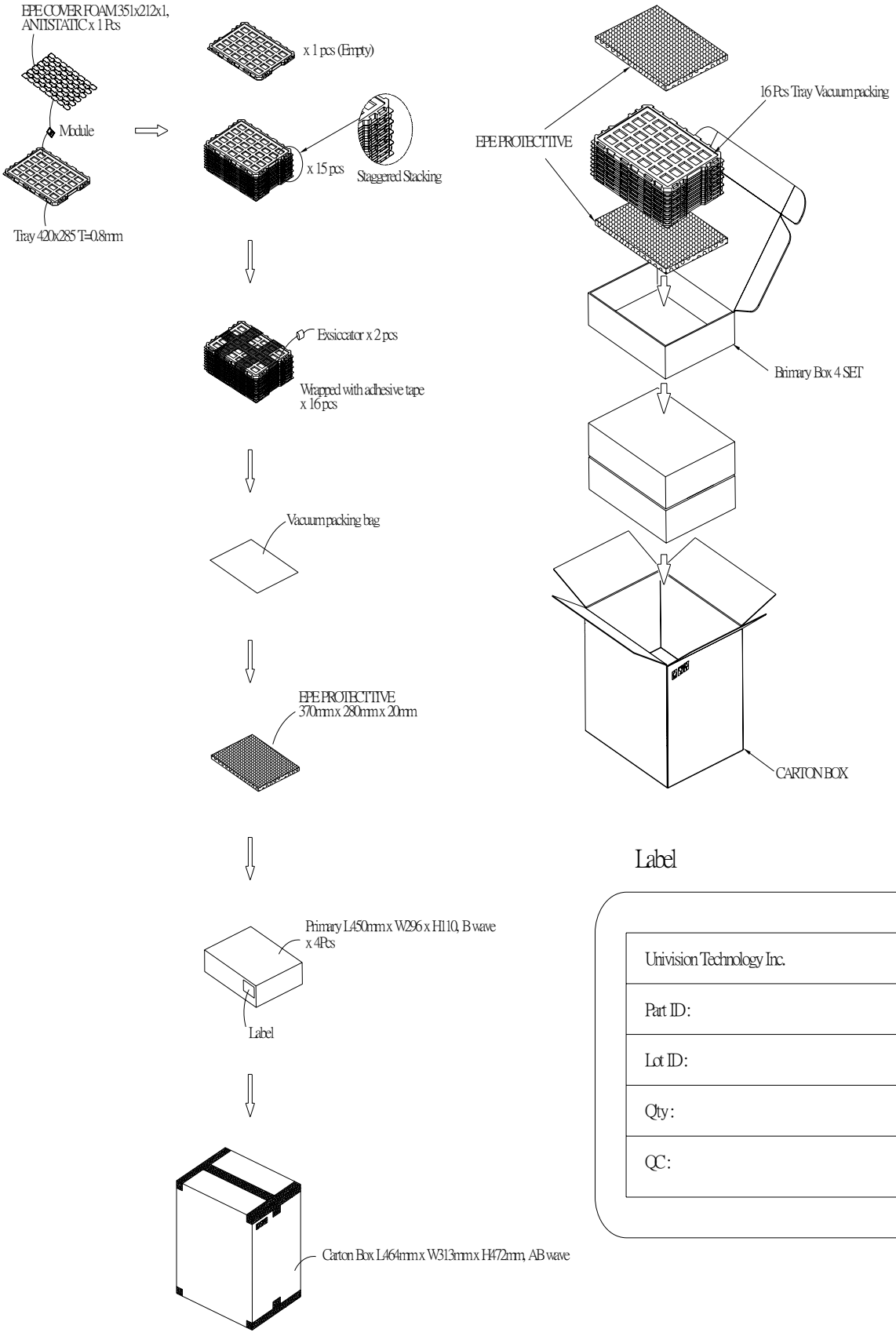




6.3.3 Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	Not allowable
Bright Line	Major	
Missed Line	Major	 
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-Uniform (Luminance Variation within a Display)	Major	

7. Package Specifications



Label

Univision Technology Inc.
Part ID:
Lot ID:
Qty:
QC:

8. Precautions When Using These OEL Display Modules

8.1 Handling Precautions

1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If pressure is applied to the display surface or its neighborhood of the OEL display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
4) The polarizer covering the surface of the OEL display module is soft and easily scratched. Please be careful when handling the OEL display module.
5) When the surface of the polarizer of the OEL display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
   * Scotch Mending Tape No. 810 or an equivalent

   Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.

   Also, pay attention that the following liquid and solvent may spoil the polarizer:
   * Water
   * Ketone
   * Aromatic Solvents
6) When installing the OEL display module, be careful not to apply twisting stress or deflection stress to the OEL display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.
7) Do not apply stress to the LSI chips and the surrounding molded sections.
8) Do not disassemble nor modify the OEL display module.
9) Do not apply input signals while the logic power is off.
10) Pay sufficient attention to the working environments when handing OEL display modules to prevent occurrence of element breakage accidents by static electricity.
    * Be sure to make human body grounding when handling OEL display modules.
    * Be sure to ground tools to use or assembly such as soldering irons.
    * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
    * Protective film is being applied to the surface of the display panel of the OEL display module. Be careful since static electricity may be generated when exfoliating the protective film.
11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OEL display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
12) If electric current is applied when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

8.2 Storage Precautions

1) When storing OEL display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps, etc. and, also, avoiding high temperature and high humidity environments or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Univision Technology Inc.)
   At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
2) If electric current is applied when water drops are adhering to the surface of the OEL display module, when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

8.3 Designing Precautions

1) The absolute maximum ratings are the ratings which cannot be exceeded for OEL display module, and if these values are exceeded, panel damage may be happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
5) As for EMI, take necessary measures on the equipment side basically.
6) When fastening the OEL display module, fasten the external plastic housing section.
7) If power supply to the OEL display module is forcibly shut down by such errors as taking out the main battery while the OEL display panel is in operation, we cannot guarantee the quality of this OEL display module.
8) The electric potential to be connected to the rear face of the IC chip should be as follows: SSPS225
   * Connection (contact) to any other potential than the above may lead to rupture of the IC.

8.4 Precautions when disposing of the OEL display modules

1) Request the qualified companies to handle industrial wastes when disposing of the OEL display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

8.5 Other Precautions

1) When an OEL display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.
   Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.
2) To protect OEL display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OEL display modules.
   * Pins and electrodes
   * Pattern layouts such as the COF
3) With this OEL display module, the OEL driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OEL driver is exposed to light, malfunctioning may occur.
   * Design the product and installation method so that the OEL driver may be shielded from light in actual usage.
   * Design the product and installation method so that the OEL driver may be shielded from light during the inspection processes.
4) Although this OEL display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.